A First-Order Noise-Shaping SAR ADC

Young Gyun Oh[1], Hyung Il Chae[a]
[1]Department of Electrical Engineering, Kookmin University
[a]Department of Electrical Engineering, Konkuk University
E-mail : [1]ohyounggyun@kookmin.ac.kr

***Abstract* – This paper presents a first-order noise shaping successive approximation register (NS-SAR) ADC with a passive residue filter. To reduce circuit complexity and increase power efficiency, the proposed NS-SAR ADC architecture uses a first-order passive integrator based on charge sharing. The attenuation coming from the charge sharing is compensated by comparator gain and first-order noise shaping is achieved totally in a passive manner, which is less sensitive to PVT variation than conventional architectures using dynamic amplifiers. In a 65-nm CMOS process, the prototype occupies 0.013 mm^2 area and consumes only 0.5 mW at sampling frequency of 150-MHz. The prototype achieves the maximum SNDR of 68 dB with oversampling ratio (OSR) of 4 and the peak value of 172.3 dB Schreier FoM (FoM$_S$).**

***Keywords*—Analog-to-digital converter (ADC), Noise shaping (NS), Successive approximation register (SAR)**

I. INTRODUCTION

The SAR ADC has good power efficiency and is suitable for IoT sensors that require moderate resolution and speed. It consists of a comparator, capacitor-DAC (C-DAC), and digital logic which is scaling-friendly. However, the resolution of the SAR ADC is often limited up to 12-bit of ENOB due to comparator noise. In order to solve the comparator noise problem, [1] proposed Majority Voting, but the proposed solution is not highly effective and increases the conversion cycles. In addition, for the high-resolution of a SAR ADC, the number of unit capacitors in the C-DAC doubles with each 1-bit increase causing increased complexity and area of the system. [2] can reduce the area by constructing a separate C-DAC to solve the increase in the area of the C-DAC when the resolution of the SAR increased. Nevertheless, due to the mismatch of C-DAC caused by the bridge capacitor, SNDR is deteriorated, requiring additional calibration circuit, which increases the complexity of the system.

A NS-SAR ADC is a hybrid ADC that has been actively studied recently. To relax the SAR ADC design, a NS-SAR ADC adopts noise shaping and oversampling technique. A SAR ADC is advantageous to implement noise-shaping easily since the error voltage remains in the C-DAC after SAR conversions. A ∑Δ ADC implements noise shaping through the loop filter for the error voltage that is the difference between the input and output voltage. Similarly, a NS-SAR ADC realizes noise shaping using a loop filter for the error voltage. The initial NS-SAR ADC [3] is implemented by using a finite impulse response (FIR) filter and an infinite impulse response (IIR) filter based on a operational-transconductance-amplifier (OTA). Although the IIR filter effectively suppresses in-band noise using the OTA, the OTA causes power consumption. The integrator of an IIR filter is implemented fully-passively in [4] to eliminate an OTA and thus to remove static power consumption. Nevertheless, due to the limitation of the passive integrator, the noise-transfer-function (NTF) was not sharp enough to effectively implement noise shaping. [5], [6] and [7] adopt a dynamic-amplifier (D-AMP) based FIR-IIR filter instead of OTA to configure sharp NTF to maximize performance. However, D-AMP is sensitive to PVT variation and requires additional calibration technology.

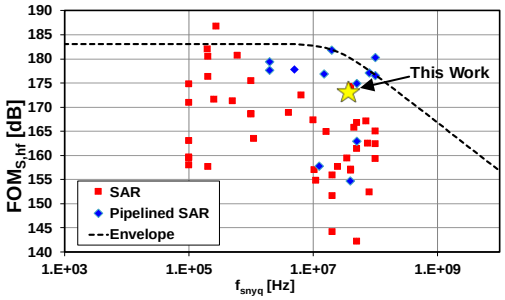


Fig. 1. Bandwidth and FoM$_S$ of SAR and Pipelined SAR.

Fig. 1 shows the relationship between FoM$_S$ and input bandwidth for recent SAR ADC designs and reveals the performance regions for SAR and Pipelined SAR [6]. FoM$_S$ represents the efficiency between resolution of ADC versus power consumption and input bandwidth. A conventional SAR ADC consists of narrow bandwidth and highest FoM$_S$ or wide bandwidth and a low FoM$_S$. A Pipelined SAR is used to realize wide bandwidth and highest FoM$_S$, but the complexity of the system is increased by the interstage-amplifier and multi-stage configuration. Our prototype constructs first-order noise shaping technique on a simple SAR structure to obtain a wide input bandwidth and large FoM$_S$ with a simple system, breaking the tradeoff between

a. Corresponding author; hichae@konkuk.ac.kr

Manuscript Received Apr. 29, 2020, Revised Jun. 25, 2020, Accepted Jun. 29, 2020

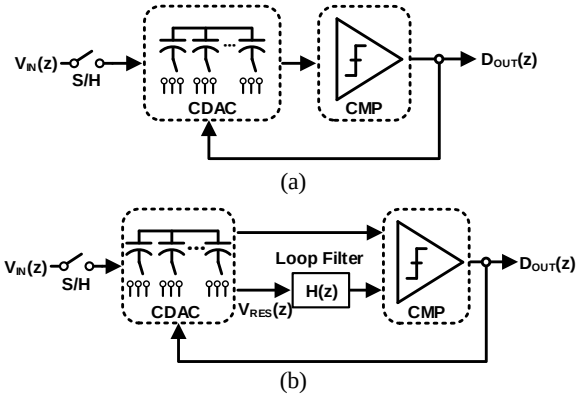


Fig. 2. (a) Conventional SAR ADC. (b) NS-SAR ADC.

input bandwidth and FoM_S.

This paper not only reduces the complexity by constructing a system with fewer switches and capacitor arrays with noise shaping technology but also makes it more robust to PVT variation. In addition, we increase the SNDR by effectively implementing noise shaping by lowering the in-band noise floor by applying the negative pole. The proposed NS-SAR ADC utilizes the comparator gain without OTA to compensate for the gain loss caused by the residue voltage (V_{RES}) integration process and reduce power consumption. The ADC prototype fabricated in 65-nm CMOS with a 1.2-V supply voltage secures 68-dB SNDR operating at 150 MS/s with only OSR of 4.

The organization of this article is as follows. Section II discusses the proposed NS-SAR ADC. Section III introduces the implementation details. Finally, we report the measured results and conclude this article in Sections VI and V, respectively.

II. PROPOSED NS-SAR ADC

A. Brief Review of NS SAR ADCs

A NS-SAR ADC implements noise shaping through the loop filter, H(z), for the error voltage of the previous step. Fig. 2 (a) shows a conventional SAR ADC structure. C-DAC samples the input voltage V_{IN}. After the sample phase, D_{OUT} is extracted by binary searching using the comparator and digital logic. Due to the structure of SAR operation, after conversions are finished, quantization error $V_{RES} = V_{IN} - D_{OUT}$ remains in C-DAC. Fig. 2 (b) shows a NS-SAR ADC. V_{RES} is combined with V_{IN} in comparator input after SAR ADC conversions through the loop filter. Through this process, the NS-SAR ADC effectively attenuates quantization and comparator noise in the in-band. The loop filter changes the in-band noise distribution. Hence, the resolution and input bandwidth of NS-SAR ADC is determined by H(z) and OSR configuration methods.

B. Prior First-Order NS SAR ADC of [9]

Passive NS-SAR ADC [10] implements summation through a multi-input comparator. However, this causes additional comparator noise, so noise shaping cannot be effectively performed. Furthermore, the comparator gain is used to compensate for the charge sharing loss, but this causes more noise. To solve this issue, [9] reduces the multi-input comparator by one through the ping-pong residue switching method and effectively reduced the noise of the comparator. Fig. 3(a) shows the simplified core schematic of the prior passive first-order NS-SAR ADC of [9]. C_{R1} and C_{R2} sample and integrate V_{RES} into C_{INT} while exchanging each other's positions for each cycle. Also, when charge sharing V_{RES} of C-DAC to C_R, it implements differential charge sharing to compensate for gain loss by realizing 2X gain. Fig. 3 (b) shows the block diagram. It consists of the cascaded of integrator feedforward (CIFF). "g" is the gain from differential charge sharing, and "a" is the gain loss that occurs when C_R and C_{INT} are charge sharing. As C-DAC and C_{INT} are connected in series, it can implement a 1-input-pair comparator. NTF is composed of first-order and consists of 1 pole and 1 zero. The zero of the NTF is configured as

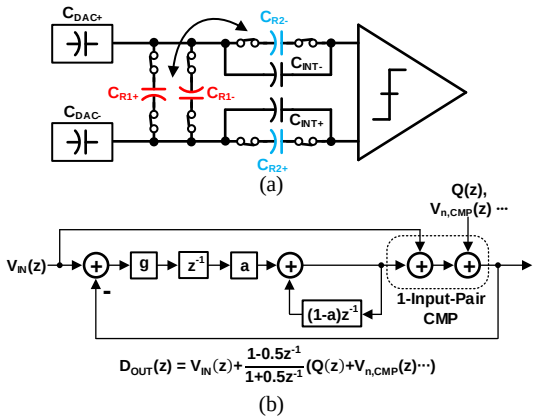


Fig. 3. (a) NS-SAR ADC using passive residue-signal summation. (b) Block diagram of NS-SAR ADC

$(1\text{-}0.5z^{-1})$ to increase the input bandwidth, and the negative pole of the NTF effectively attenuated in the in-band noise, maximizing the efficiency over the normal noise shaping. However, [9] has a complicated switching process to implement ping-pong structure, which causes parasitic capacitance, thus reduces DR and leads to the additional gain loss in the charge sharing process. Besides, to configure as a 1-input-pair comparator, C-DAC and C_{INT} adopt the serial connection, and more errors occur due to kickback. It is also the mismatch of C-DAC, C_R, and C_{INT} cause the position of the pole and zero of NTF can be changed.

C. Proposed First-Order NS-SAR ADC

The architecture of the proposed first-order NS-SAR ADC is shown in Fig. 4 (a). Although the real implementation is fully differential, a single-ended version is shown here for simplicity. C-DAC is composed of 10-bit and operated with asynchronous SAR logic for fast operation. In order to improve switching power efficiency, power consumption is reduced by performing MCS based switching [11].

Although bottom-plate sampling prevents the charge injection of the sampling switch and distortion, it is difficult for the sampling switch resistance to be linear. So, the

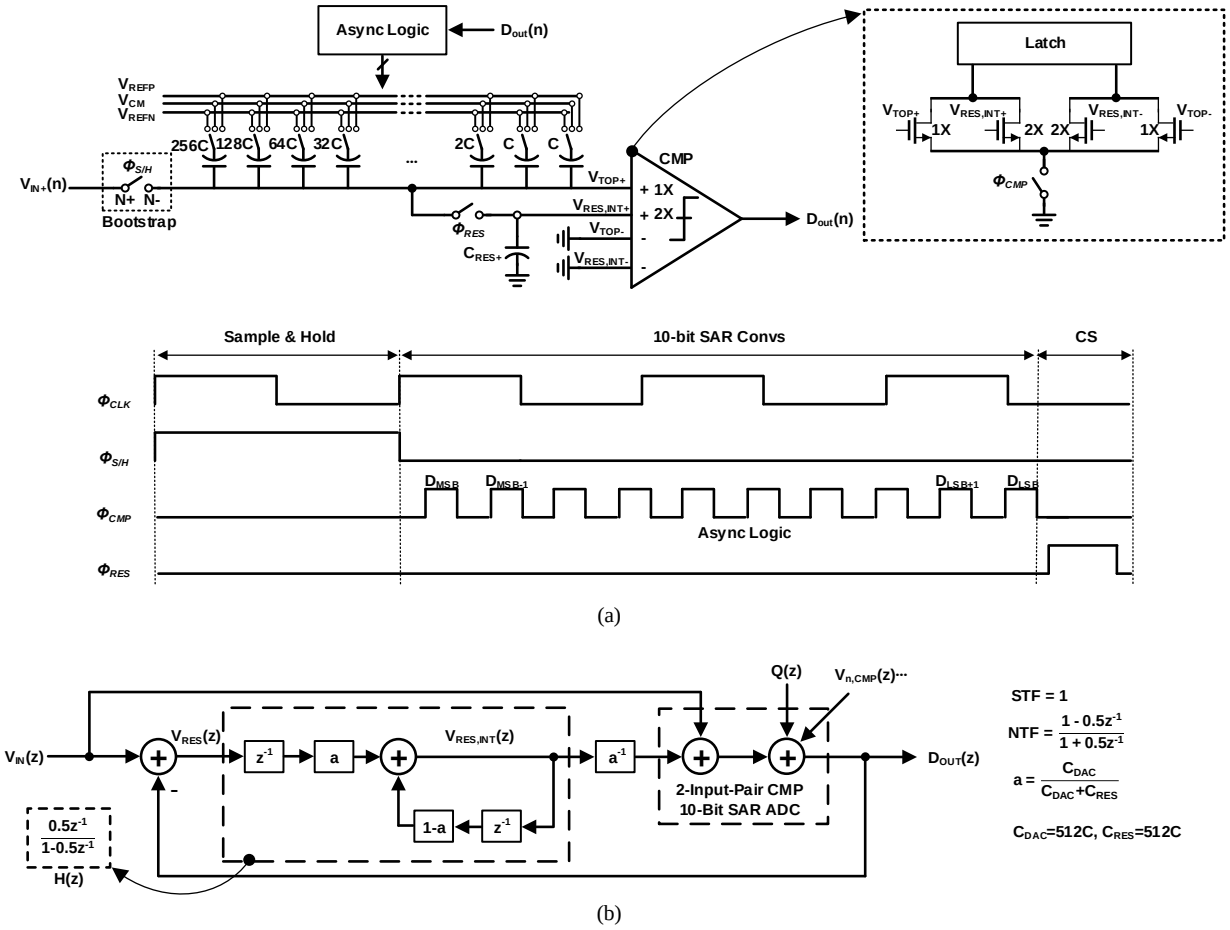


Fig. 4. (a) Proposed first-order passive NS-SAR architecture and timing. (b) Signal flow diagram of the proposed NS-SAR ADC.

settling issue causes harmonics. Therefore, C-DAC performs sampling using a bootstrap circuit while performing the top-plate sampling. More details will be given in Section III.

One switch and capacitor arrays are added to implement the first-order NS-SAR ADC. C_{RES} is used as a passive integrator while sampling residue voltage. The integrated residual voltage, $V_{RES,INT}$, is inserted into the comparator input for the next conversion to implement noise shaping. The comparator also implements the 2-input-pair configuration and is used as analog summing as well as 2X gain to compensate for integration loss. Although comparator noise has increased by using multi-input and comparator gain, it can reduce the noise by limiting the bandwidth and does not significantly affect the SNR by the first-order noise shaping effect. The comparator is composed of a double tail latch type, and the gain is realized by using the multiplier. It will be described in detail in Section III.

Fig. 4 (b) is a z-domain diagram of the proposed NS-SAR ADC signal flow. The proposed structure is the CIFF structure, assuming $C_{DAC} = C_{RES} = 512C$ and $a = C_{DAC} / (C_{DAC} + C_{RES})$. The path at the top of the comparator input stage is the $V_{IN}(z)$ signal for normal SAR operation. When $\Phi_{S/H}$ is high, the input voltage is sampled on the C-DAC. After sampling, 10-bit asynchronous logic operates. $D_{OUT}(z)$ is the output value of the ADC, so it becomes $V_{RES}(z) = V_{IN}(z) - D_{OUT}(z)$. When Φ_{RES} is high after the last data output, D_{LSB}, is over, C-DAC and C_{RES} charge sharing, and V_{RES} is integrated into the C_{RES} with the V_{RES} of the previous step. "a" occurs due to charge sharing loss. So the loop filter is

$$H(z) = \frac{V_{RES,INT}(z)}{V_{RES}(z)} = \frac{az^{-1}}{1 - (1 - a)z^{-1}} \quad (1)$$

The pole of the first-order integrator is located at "(1-a)". The comparator gain "a^{-1}" is used to compensate for integration loss "a". $V_{IN}(z)$ and filtered V_{RES}, $H(z)V_{RES}(z)$, are combined in a 2-input-pair comparator and quantized. Through the final analog-to-digital conversion process, $D_{OUT}(z)$ is represented by the sum of $H(z)V_{RES}(z)$, $V_{IN}(z)$, and Q(z). Using the signal flow diagram, one can obtain the complete z-domain transfer function of the ADC

$$\begin{aligned} D_{OUT}(z) &= V_{IN}(z) + \frac{Q(z)}{1 + a^{-1}H(z)} \\ &= V_{IN}(z) + \frac{1 - (1 - a)z^{-1}}{1 + az^{-1}}Q(z) \end{aligned} \quad (2)$$

which clearly shows the first-order noise shaping. $V_{n,CMP}(z)$, etc., noises, which are the same input path as Q(z), also are implemented noise shaping.

As shown in (2), the value of "a" determines the location

of the pole and zero of the NTF. To realize effective noise shaping, a negative pole must be used. Therefore, "a" was implemented as 0.5 to effectively suppress the in-band noise. Unlike the NTF ($1-z^{-1}$) of the conventional first-order noise shaping, the proposed structure has a zero at 0.5 to form a wide input bandwidth. Our structure is constructed with a simple structure while realizing the same NTF as [9] and designed to be robust to PVT variation. We reduce the complexity of the circuit by using a fewer number of switches, capacitor arrays, and adopting comparator gain rather than an OTA-based IIR filter.

III. IMPLEMENTATION DETAILS

A. Multi-Input Comparator

NS-SAR ADC based on an OTA causes power-hungry. To reduce power consumption, we increase power efficiency by using the comparator gain. Fig. 5 represents the comparator structure of the double-tail latch-type [3]. In Fig. 4(b), to sum V_{IN} and filtered V_{RES}, the comparator is composed of multiple inputs. Moreover, the input of the V_{TOP} is 1X and the input of the $V_{RES,INT}$ is 2X, so the gain is easily realized. Assume the transconductance of the input MOSFET is g_m, it becomes $I_{SUM}=(V_{TOP}+2V_{RES,INT})g_m$, and amplification and summation are implemented simultaneously.

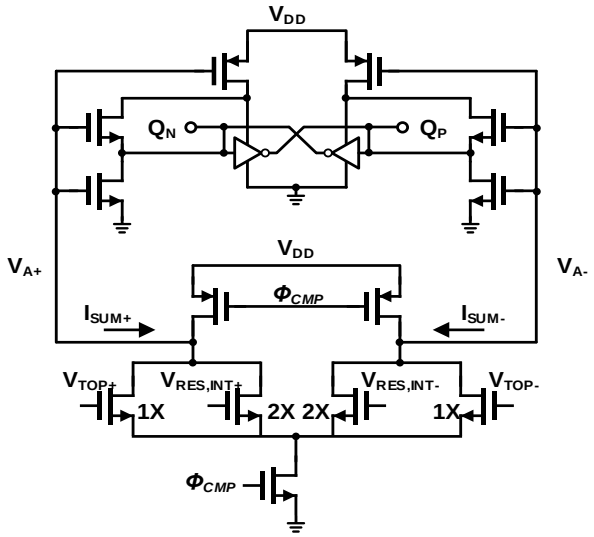


Fig. 5. Multi-input double-tail comparator

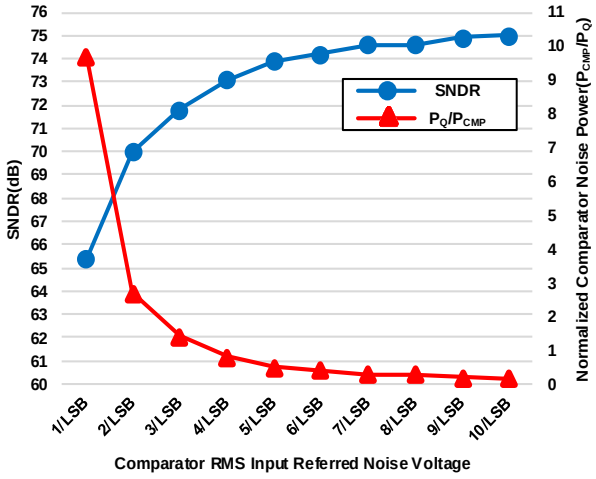


Fig. 6. Comparator noise versus normalized comparator noise to quantization noise and SNDR

When Φ_{CMP} is high, V_{TOP} and $V_{RES,INT}$ are combined in the form of current, respectively, and Q_N and Q_P values are determined by latch operation according to the voltage difference of the V_A node. When Φ_{CMP} is low, each node of the comparator is initialized.

The input-referred noise of a comparator should be minimized to achieve desired the NS-SAR ADC performance. Fig. 6 represents the SNDR versus the noise of the input-referred comparator noise ($V_{n,CMP}$) based on the LSB, and the power obtained by normalized the input-referred comparator noise power (P_{CMP}) to the quantization noise power (P_Q). The proposed structure is 2.4 V for full-scale range and 2.3 mV for 1LSB based on 10-bit SAR ADC. It has good performance when $V_{n,CMP} < LSB/6$, but $V_{n,CMP}$ is designed on LSB/3 considering the comparator's bandwidth and power consumption. A comparator input-referred noise can obtain through cross-validation of PSS engine and transient noise simulation.

B. Bootstrapped switch

The bootstrapped switch [12] shown in Fig. 7 performs the sampling function. Using a general transmission gate switch does not guarantee linearity, which generates more harmonics. To overcome this issue, we choose the bootstrapped switch circuit. It ensures linearity by making the $V_{GS}(= V_{GATE} - N+)$ of MN_0 a constant voltage with V_{DD}. When Φ_{SW} is low, V_{DD} is charged to C_{BOOT}, and when Φ_{SW} is high, the gate of MN_0 moves to $V_{IN} + V_{DD}$ to form a low and constant switch resistance R_{ON}. The body contact of MP_0 and MP_1 is constructed as shown in Fig. 7 to prevent forward bias of pn-junction. Besides, if C_{PAR1} and C_{PAR2} are large, the linearity of the bootstrap switch cannot be guaranteed, so they should be minimized. Hence, C_{BOOT}, which consists of a metal-oxide-metal (mom) capacitor, should employ the upper metal layer rather than the lower metal layer to minimize parasitic capacitance from the substrate.

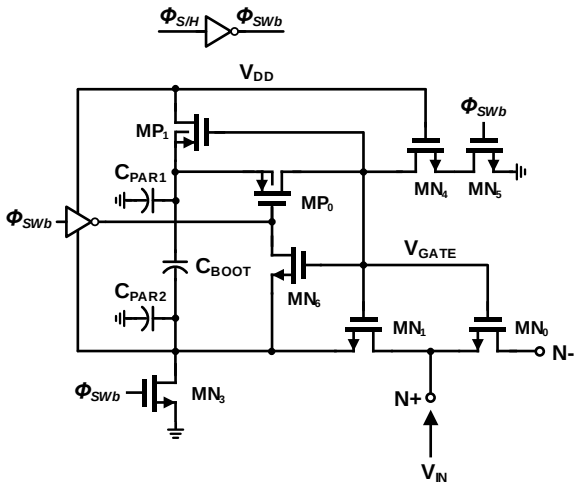


Fig. 7. Bootstrap circuit

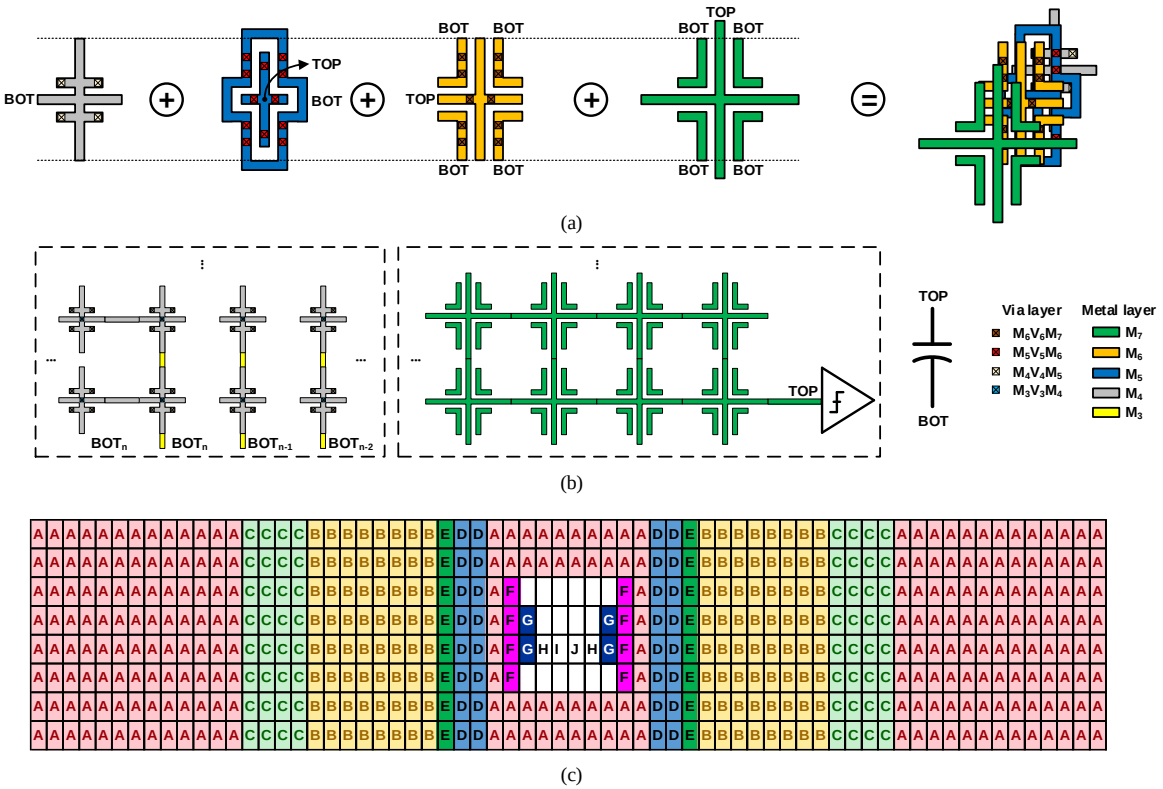


Fig. 8. (a) Proposed unit capacitor structure. (b) Example of a C-DAC. (c). The layout floorplan of the capacitor array.

C. Proposed C-DAC structure

In order to reduce the switching power, the unit capacitor (C_{unit}) must be reduced. The proposed C_{unit} of NS-SAR ADC is designed with custom mom capacitor. The switching power is effectively decreased by configuring the C_{unit} as 1.25fF. Fig. 8 (a) shows a C_{unit} consisted of M_5 to M_7. The M_4 is placed for wire routing between the bottom plates (BOT) of the C_{unit}. Each metal is constructed at a minimum distance to form the maximum capacitance between the top plate (TOP) and the BOT. By shielding the TOP with the BOT, thereby unnecessary parasitic capacitance is minimized to prevent a mismatch. V_4 to V_6 connected the upper metal and the lower metal. Fig. 8 (b) is an example of a C-DAC. The routing of the TOP applied to the comparator input is connected to the M_7 to minimize parasitic capacitance with the substrate. The BOT, which is connected to the reference switch, effectively routed the M_3 in the vertical direction and the M_4 in the horizontal direction. Fig. 8 (c) shows the floorplan of the layout of the capacitor array. The MCS switching method of 10-bit SAR ADC requires 512 unit capacitors. C-DAC can be designed with a common centroid layout, but since the value of C_{unit} is considerably small, if the complexity of the routing increases, mismatch more occurs, so it cannot guarantee linearity. Therefore, we optionally mix and arrange C-DAC arrays. The empty space and outline are filled with a dummy to minimize gradient mismatch.

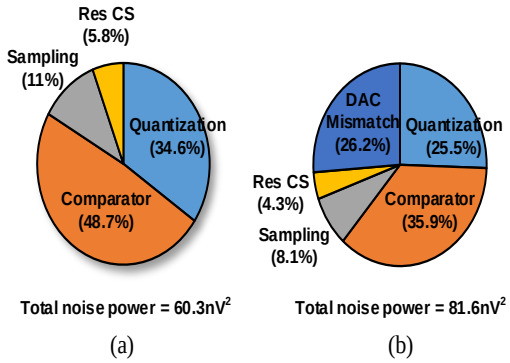


Fig. 9. Calculated in-band noise breakdown of the prototype ADC (a) Except C-DAC mismatch (b) Include C-DAC 0.5% mismatch

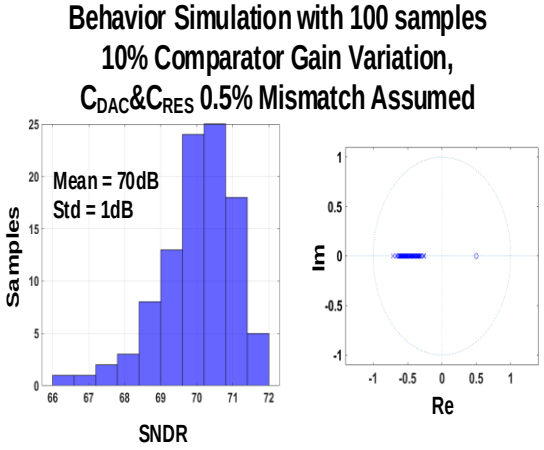


Fig. 10. Capacitor mismatch and comparator gain variation effects

D. Noise and C-DAC Mismatch Design Considerations

Fig. 9 shows the in-band noise breakdown of the prototype NS-SAR ADC. Fig. 9 (a) shows that the largest noise source is the comparator. Residue charge sharing (Res CS) is a noise that occurs when C-DAC and CRES are connected and do not take a large part. Another concern about the design is the linearity, which is mainly affected by the capacitor mismatch of the C-DAC. Fig. 9 (b) is the noise portion when C-DAC 0.5% mismatch occurs. Through the parasitic extraction simulation, the mismatch ratio of C-DAC except gradient mismatch is found to be 0.5%.

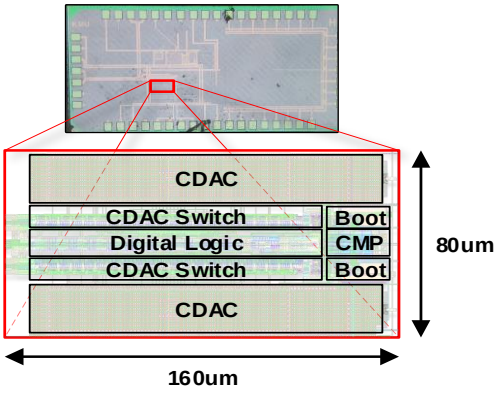


Fig. 11. Chip micrograph of the proposed NS-SAR ADC and layout of the ADC core

E. PVT Considerations

PVT variation is an important effect that affects ADC performance. However, the performance of the proposed NTF is determined by the ratio of capacitors and the comparator transistor sizes. As shown in (2), C_{DAC}, C_{RES} size, and comparator gain affect pole location. Zero is only determined by the capacitor size ratio. The gain change of the comparator depends on the common-mode and the differential-mode gain, but the common-mode change does not significantly influence within a reasonable range. The comparator gain has a 10% gain variation through the Monte Carlo Simulation results. The capacitor is 0.5% mismatched through the results of parasitic extraction simulation. Fig. 10 shows the behavior simulation, including extracted capacitor mismatches, comparator gain variations, and calculated in-band noise. The proposed structure is a stable system because the poles exist in the unit circle. The zero is a parameter determined simply by the capacitor, so its effect is small and does not change if the parasitic component is small. With these features, our structure has PVT robust.

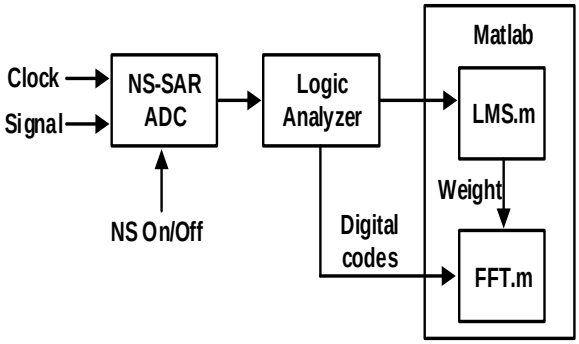


Fig. 13. Off-chip foreground calibration implementation.

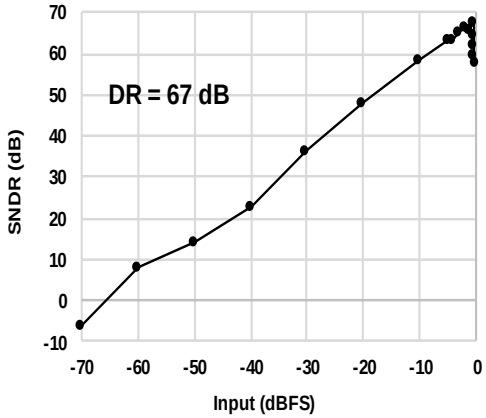


Fig. 14. Measured SNDR versus input power

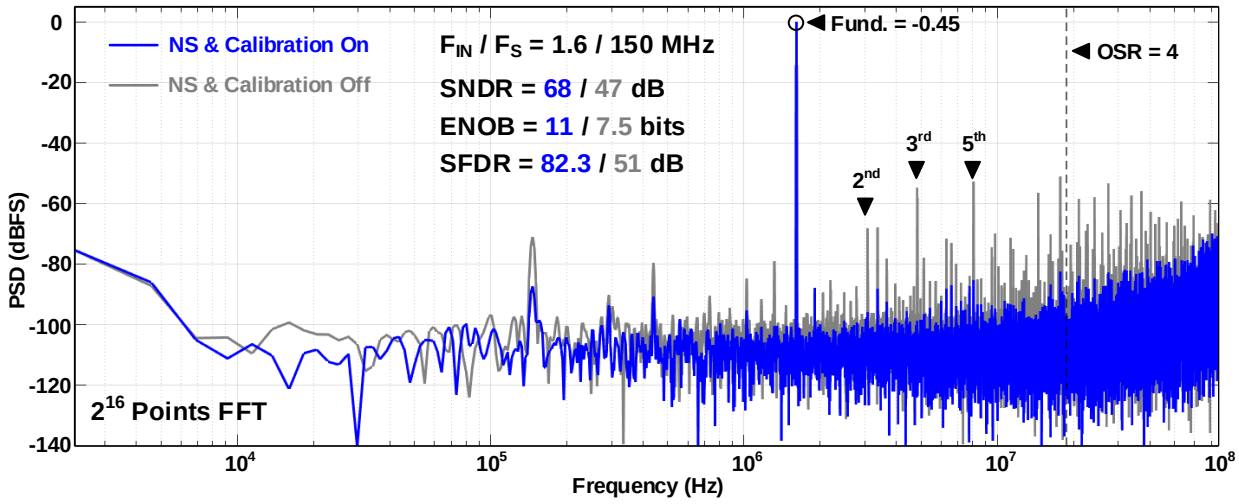


Fig. 12. Measured output PSD for different configurations.

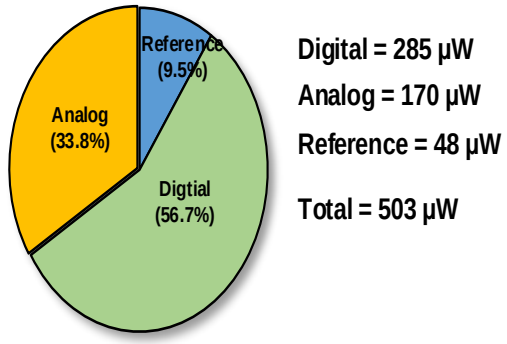
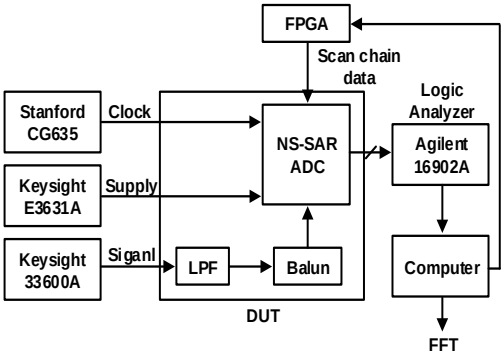


Fig. 15. Measured power breakdown

(a) NS-SAR ADC verification setup



(b) Test environment block diagram

Fig. 16. NS-SAR ADC DUT environment and peripherals block

VI. MEASUREMNTS

The prototype NS-SAR ADC is fabricated in 65-nm CMOS and has an active area of 0.013 mm^2. The maximum sampling rate is 150 MS/s and with an OSR of 4; the effective bandwidth is 18.8 MHz. Fig. 10 shows a chip photograph. Fig. 11 shows the measured FFT at 150 MS/s, indicating a peak SNDR of 68 dB. It shows the comparison of the performance when the noise shaping is running, the calibration is enabled and disabled. The internal buffer generates the reference voltages V_{REFP} and V_{CM}.

Fig. 13 shows the process of implementing the foreground calibration. The mismatch error is calibrated in the foreground by least-mean-square (LMS) algorithm. Calibration compares the standard codes without linearity error and the output data codes of the ADC when performing normal SAR operation, and obtains the bit weight of the DAC through the LMS iteration process. At the end of the LMS iteration, the final ADC digital output is obtained by updating the actual bit weight to the NS-SAR's DAC. Off-chip calibration requires a once calculation process. Once we find the DAC weight, we don't need any further calibration.

It can be seen that the CDAC mismatch has occurred significantly. Mismatch occurs largely due to the appearance of a custom capacitor rather than a conventional finger type mom capacitor. Also, a routing mismatch worsens more than the result of post-extraction.

The measured performance versus input amplitude is presented in Fig. 14, showing a dynamic range (DR) of 68 dB.

At the supply voltage of 1.2 V, the chip power consumes in total 503 μW, out of which 285 μW comes from digital circuits such as SAR logic, clock generator, and buffer, 170 μW comes from the analog circuit comes from the comparator and comparator logic, and 48 μW comes from the DAC switching, as shown in Fig. 15. Although our prototype has reduced the reference power using the implementation of MCS based switching, we can see that digital power has increased due to the additional switches and digital circuits.

Fig. 16 shows the NS-SAR ADC test environment.

IV. CONCLUSION

This paper proposes first-order NS-SAR ADC that is robust to PVT variation and simple. It decreases the complexity of the circuit with a few switches and capacitor arrays. Moreover, a sharp NTF was constructed without OTA using the comparator gain and the negative pole. We propose a circuit that is easy to implement with the same NTF compared to [9]. The ADC prototype draws 0.5 mW power from a 1.2-V supply at a conversion rate of 150 Ms/s and exhibits FoM_S 172.3 dB with only OSR of 4.

ACKNOWLEDGMENT

This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Science and ICT(No. 2018R1D1A1B07048794). Chip fabrication and EDA tools were partially supported by the IDEC, Korea.

REFERENCES

[1] Harpe, Pieter, Eugenio Cantatore, and Arthur van Roermund. "A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1 b ENOB at 2.2 fJ/conversion-step.", IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3011-3018, Dec.2013

[2] Yoshioka. M, "A 10b 50MS/s 820uW SAR ADC with on-chip digital calibration.", 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2010

[3] Fredenburg, Jeffrey A., and Michael P. Flynn, "A 90-ms/s 11-mhz-bandwidth 62-db sndr noise-shaping sar adc.", IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 2898-2904, Dec.2012

[4] Zhijie Chen, Masaya Miyahara, and Akira Matsuzawa,

"A 9.35-ENOB, 14.8 fJ Fully-Passive Noise-Shaping SAR ADC", Symposium on VLSI Circuits, 2015
[5] Liu, Chun-Cheng, and Mu-Chen Huang, "28.1 A 0.46 mW 5MHz-BW 79.7 dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter.", IEEE International Solid-State Circuits Conference (ISSCC). IEEE, 2017.
[6] Miyahara, Masaya, and Akira Matsuzawa. "An 84 dB dynamic range 62.5–625 kHz bandwidth clock-scalable noise-shaping SAR ADC with open-loop integrator using dynamic amplifier.", IEEE Custom Integrated Circuits Conference (CICC). IEEE, 2017.
[7] Li, Shaolan, et al, "A 13-ENOB second-order noise-shaping SAR ADC realizing optimized NTF zeros using the error-feedback structure.", IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3484-3496, Dec.2018
[8] B. Murmann. ADC Performance Survey 1997–2018. Accessed: May 10, 2019. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html
[9] Lin, Ying-Zu, et al, "20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC With Passive Signal-Residue Summation in 14nm FinFET.", IEEE International Solid-State Circuits Conference-(ISSCC). IEEE, 2019.
[10] Guo, Wenjuan, Haoyu Zhuang, and Nan Sun, "A 13b-ENOB 173dB-FoM 2 nd-order NS SAR ADC with passive integrators.", symposium on VLSI circuits. IEEE, 2017.
[11] Hariprasath, V., et al, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency.", Electronics letters, vol. 46, no. 9, April.2010
[12] Liu, Chun-Cheng, et al, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure.", IEEE Journal of Solid-State Circuits, vol. 45, no. 4, pp. 731-740, April.2010

Young Gyun Oh received the B.S. degree in electronic engineering from Kookmin University, Seoul, Korea, in 2019. He is currently working toward the M.S. degree in electrical engineering at Kookmin University. His research during the M.S. course has focused on analog to digital converter.

Hyung Il Chae received his B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2004, and his M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2009 and 2013, respectively. From 2013 to 2015, he was a senior engineer at Qualcomm Atheros, San Jose, CA, USA. From 2015 to 2019, he was a associate professor at Kookmin University, Seoul, South Korea. He joined Konkuk University, Seoul, South Korea, in 2019, and is currently an associate professor. His research interests include mixed signal and RF circuit design. Dr. Chae is the recipient of a KFAS Fellowship.