Design of a Continuous-Time Delta-Sigma Modulator for Bio-signal Acquisition

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***Abstract* - This work presents a design methodology of a low-noise and low-power continuous-time delta-sigma modulator (CT DSM) architecture for bio-signal acquisition. Along with the 2nd-order CT loop filter architecture, a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) is used as a quantizer to achieve power efficiency. The incremental operation is added to enable multi-channel processing. Designed and fabricated in a 180nm CMOS process, the proposed architecture achieves 80.1dB SNDR in a 250kHz bandwidth (BW) under a 1.8V supply. With a power consumption of 2mW, the proposed architecture has a Schreier Figure of Merit (FoMs) of 161dB.**

***Keywords*—Analog-to-Digital Converter (ADC), Continuous-Time (CT), Delta-Sigma Modulator (DSM)**

I. INTRODUCTION

The field of medical and engineering technology has experienced significant advancements, resulting in the expansion of the range of usable bio-signals and rapid development of bio-signal processing technology. Bio-signals, which encompass electrical signals obtained from electrodes such as ECG (Electrocardiogram), EMG (Electromyogram), and EEG (Electroencephalogram), exhibit varying electrical properties such as amplitude and frequency range. Analyzing the electrical properties of these bio-signals has numerous potential applications, including disease prevention and investigation through implantable medical devices or brain-device interfaces. However, to analyze these bio-signals, an analog-to-digital converter (ADC) is required to convert the signals into digital domain as they are analog signals that require digital processing. The performance of the ADC is critical, as the ADC quantization noise dominates the noise performance of the analog front-end (AFE) circuits of the bio-signal acquisition system.

To convert a bio-signal to a digital signal, the speed of the converter doesn't need to be particularly fast, since bio-signals typically have relatively low frequency ranges, usually up to around 10kHz. However, a low-noise level is essential for detecting small signal amplitudes. Additionally, as multiple electrodes are typically used to collect bio-signals, multi-channel processing is required.

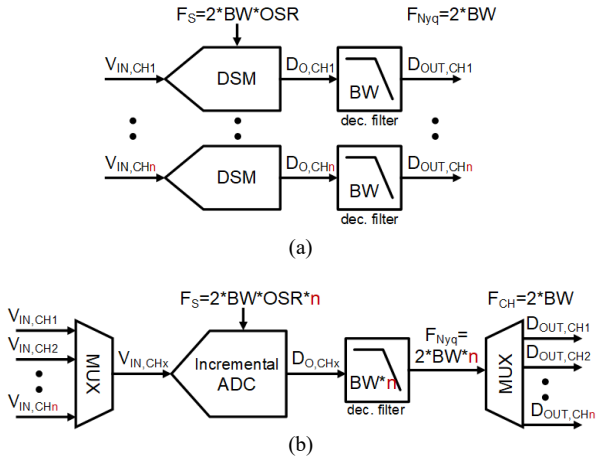

Fig. 1. Multi-channel processing ADC using (a)multiple parallel ADC and (b)single fast ADC.

The low-noise multi-channel processing can be done with two methods as shown in Fig. 1. First is to use multiple parallel ADCs with a slow conversion rate (Fig. 1(a)). This approach offers the benefit of allowing each single ADC to have a slow speed. However, the use of large passive components can degrade the integrator amplifier performance, and transistor flicker noise can also degrade the noise performance. Using this multiple parallel architecture, it is challenging to design the ADC as low-power and low-noise in a compact area-efficient circuit.

Next is to use one fast ADC with a conversion rate of a multiple of the number of channels, along with the multiplexers (MUXs) (Fig. 1(b)). In this bio-signal acquisition system requiring low noise, Delta-Sigma Modulator (DSM) architecture is necessary. Indeed, traditional DSM architecture is not suitable for multiplexed environments. In this case, an incremental operation is needed for the DSM to be used in multi-channel processing.

To achieve an inherent anti-aliasing effect, the incremental architecture for Delta-Sigma Modulators (DSMs) has been implemented using continuous-time (CT) architecture [1]-[2], as opposed to the conventional discrete-time (DT) approach [3]. This CT approach has recently been used for low-noise multi-channel processing, but there are only a limited number of studies on this architecture, indicating that

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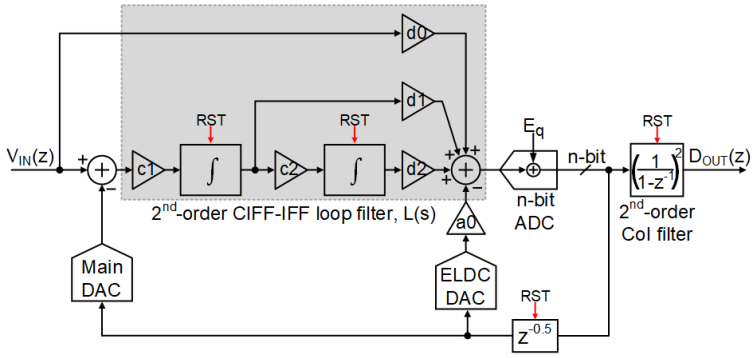


Fig. 2. Block diagram of the proposed CT DSM.

there is still significant potential for improvement in this area.

This work introduces a low-noise and low-power ADC architecture for implantable bio-signal acquisition system. A 2nd-order Continuous-Time Delta-Sigma Modulator (CT DSM) with 250kHz bandwidth (BW) is designed, which can be utilized in multi-channel processing using incremental operation. Incremental mode enables the ADC to have maximum output rate of 500kS/s.

Section II shows the design methodology of the bio-signal acquisition ADC. Section III presents the detailed circuit implementations and simulation methods. Section IV shows the measurement results, and section V concludes the paper.

II. DESIGN METHODOLOGY

A. Design Considerations

To achieve a low noise level in an ADC, the use of DSM architecture is desirable as it operates with oversampling and noise-shaping techniques to minimize in-band noise. However, this noise-shaping technique does not apply to the input noise, such as front-end noise and thermal noise at the ADC input. Therefore, front-end noise reduction is also necessary for a low-noise design. In this regard, the CT DSM architecture has an advantage due to its inherent anti-aliasing property.

In order to achieve low power consumption, it is advantageous to minimize the number of active amplifiers as they typically consume a significant amount of power. One approach to reducing the number of amplifiers is to use a multi-bit quantizer to decrease the quantization noise along with low loop filter order. Employing a multi-bit ADC not only leads to a reduction in quantization noise, but also relaxes the design constraints on amplifiers. The Successive Approximation Register (SAR) ADC is a good choice for this purpose as it is an energy-efficient architecture. Use of an SAR ADC would result in further in-band noise reduction while maintaining power efficiency.

Another consideration is the use of a single ADC for multi-channel processing, as the implementation of multiple parallel ADCs may be limited by area constraints. Since general DSM architecture does not offer sample-by-sample conversion, an incremental operation is required. By applying incremental operation, one-to-one mapping between input and output enables multiplexing of the DSM architecture.

B. Proposed Architecture

Fig. 2 depicts the block diagram of the proposed CT DSM. A 2nd-order CT loop filter is chosen to minimize the number of amplifiers while simultaneously ensuring a high Signal-to-Quantization Noise Ratio (SQNR). Cascade of Integrators Feed-Forward (CIFF) with input feed-forward (IFF) structure is utilized as it exhibits low noise and distortion when referred to the input, and it also necessitates fewer feedback Digital-to-Analog Converters (DACs). To account for the conversion time of the SAR ADC and data-weighted averaging (DWA), the excess loop delay (ELD) is set to $0.5T_S$ (equivalent to a half clock cycle), represented by $z^{-0.5}$ in the block diagram. Accordingly, the ELD compensation (ELDC) DAC is also added at the input of the quantizer.

To enable incremental operation, an additional periodic reset (RST) operation and a simple Cascade of Integrators (CoI) digital decimation filter can be used. Since the loop filter is designed to produce 2nd-order shaped quantization noise (Eq), the CoI decimation filter should also be designed as 2nd-order to match the order of the loop filter.

C. System-level Verification

To meet the design requirements by considering the design variables, the proposed architecture was modeled and simulated in MATLAB. Fig. 3 (a) shows the Simulink model of the system-level architecture created utilizing the MATLAB toolbox [4]. The toolbox was used to simulate the multi-bit ADC and evaluate the power spectral density (PSD) for determining the SQNR. Periodic reset operation for incremental function can be applied to all components with memory effect, such as the loop filter and decimation filter.

Both the first and second integrators are set to be in the CT domain, with the transfer function of $k1/s$ and $k2/s$, respectively. The coefficients $k1$ and $k2$ are equal to 1 in the normalized domain and should be set to sampling frequency, F_S, when simulating the system with a specific sampling frequency. Coefficients of the behavioral model are set to factors considering DT-to-CT conversion using impulse invariance, input scaling, dynamic range scaling, and ELD compensation to avoid integrator saturation. The coefficients are generated by the synthesis tool [5] and adjusted to fit the requirements.

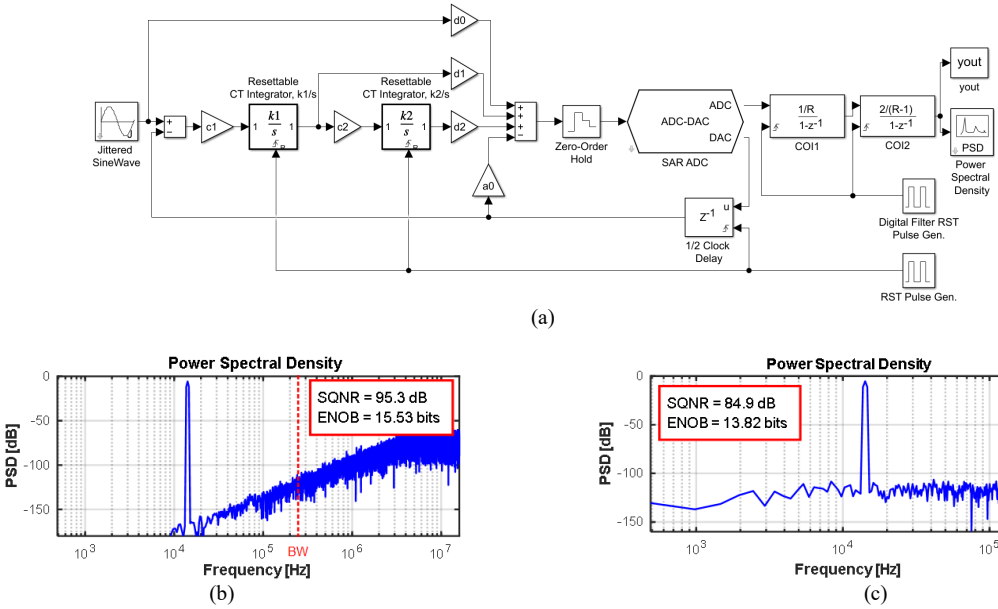


Fig. 3. System-level verification: (a) test setup in MATLAB Simulink, (b) simulation result in DSM mode, and (b) incremental mode.

The model was simulated using the obtained coefficients to determine the appropriate oversampling ratio (OSR) and the resolution of the SAR ADC required to meet the low-noise requirement. Fig. 3 (b) and (c) show the simulated results of the ideal CT DSM in DSM mode and incremental mode, respectively. The CT DSM achieves an SQNR of 95dB in DSM mode and 85dB in incremental mode with an OSR of 64 and a 4-bit ADC. The incremental mode exhibits a 10dB reduction in SQNR compared to the DSM mode, due to the loss of information in the loop filter during the reset operation. Although this performance difference can be alleviated by reducing the OSR or changing the NTF, the OSR and the NTF are set to meet the target SQNR performance. With 32MHz system clock (F_S), the maximum Nyquist conversion rate of this single ADC is set to 500kS/s. In a multiplexed environment, for instance, if a signal has a BW of 15.625kHz, the designed ADC allows multiplexing of up to 16 channels.

III. IMPLEMENTATION

A. Loop Filter and DAC

Simplified circuit implementation is shown in Fig. 4 (designed in differential mode). Active-RC integrators are used for the CT DSM loop filter to ensure high linearity. The 1st integrator is configured with R_{INT1}, C_{INT1}, and AMP1, while the capacitor C_{FF} implements the 1st integrator's output feed-forward path. The 2nd integrator consists of R_{INT2}, C_{INT2}, and AMP2. A two-stage Miller-compensated op-amp is used for both integrators, with AMP1 designed to drive the resistive load of the 2nd integrator, and AMP2 designed to have a high output swing range. The low-distortion input feed-forward path is implemented through a capacitive coupling path at the input of AMP2 using C_{IFF}.

Main feedback DAC is implemented as Resistor DAC (RDAC) to minimize noise. The total resistance of the

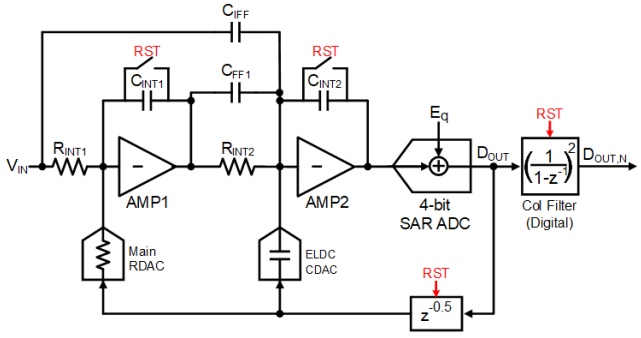


Fig. 4. Circuit Implementation of the proposed ADC.

RDAC, $R_{DAC,total}$, is equal to that of R_{INT1} to implement a path gain of 1. For excess loop delay compensation (ELDC), a Capacitive DAC (CDAC) is applied to the AMP2 summing node, reducing power consumption compared to using an extra summing op-amp. The total capacitance of this CDAC is $C_{ELDC,total}$.

The values of the passive RC components used in the loop filter need to be assigned based on the coefficient obtained from the MATLAB simulation, as presented in Table I. Since the value of R_{INT1} should be selected based on the thermal noise limit, the values of other passive components will be determined accordingly.

B. Simulation for Thermal Noise-limited Design

The in-band noise of a CT DSM contains thermal noise and shaped quantization noise. For a power-efficient design, it is recommended to select a thermal noise-limited design, as reducing quantization noise requires less power [6]. The general guideline is to keep the quantization noise at least 10-12dB lower than the thermal noise. This would be beneficial as quantization could also contain harmonics.

The thermal noise in CT DSM is dominated by R_{INT1}, R_{DAC}, and AMP1 transistor noise, as the thermal noise

behind the 1st integrator will be attenuated by the front-end gain. Since the values of passive components should be fixed before the design of the amplifier, R_{INT1} can be first selected by running the transient noise simulation in the ideal model. This is important as the thermal noise in voltage-input DSM is directly proportional to the size of the input and feedback DAC resistors (equivalent to $8kTR$).

Using the ideal model simulation in cadence, we can inspect the thermal noise floor contributed by R_{INT1} and R_{DAC} and set the appropriate noise target. The ideal model should be created to operate with the same clock and logic, but using an ideal amplifier, ideal passive components, and an ideal quantizer. First, the resistance value is roughly set. Before running the transient analysis with noise, we can choose to include the noise contribution only by the input and feedback DAC resistors. By running this simulation several times and allowing it to have a noise limit of around 10dB above the quantization noise floor, R_{INT1} and R_{DAC} can be selected accordingly. Subsequently, the AMP1 is also designed to have targeted thermal and flicker noise. The chopping technique can be applied if the flicker noise dominates the targeted thermal noise performance.

C. Multi-bit Quantizer

A SAR ADC is utilized as the 4-bit quantizer. A binary-weighted CDAC is utilized, and the bottom switch of the CDAC is simply implemented using an inverter owing to top-plate sampling and split-capacitor switching [7]. A strong-arm latch is used for the comparator. Since most of the quantizer noise is shaped by the loop filter, the design requirements of the SAR ADC, such as kT/C sampling noise and comparator noise, are much more relaxed. Asynchronous SAR control logic is selected to eliminate the need for an extra fast clock. The output of the quantizer passes through rotational DWA logic before the feedback to the DAC after the ELD.

D. Decimation Filter for Incremental Operation

To simply evaluate the performance of a general DSM, a physical decimation filter is not required as we can ideally evaluate the performance only considering the in-band signal and noise components (equivalent to ideal filtering of the out-of-band signals). However, as incremental operation results in a finite impulse response (FIR) system due to periodic reset, an FIR filter is required. The CoI filter is the simplest and most effective FIR filter utilized for incremental ADC. Fig. 5 shows the implementation of this CoI filter with a DSM output of 4 bits with an OSR of 64. The first digital integrator has a maximum 10-bit output (4b input, 2^6 OSR), and the second digital integrator has a maximum 16-bit output (10b input, 2^6 OSR). The CoI filter (2nd order digital integrator) can be simply implemented with an adder and a D-flipflop (D-FF) per bit.

E. Simulation for Overall Performance Evaluation

After each circuit block is designed and verified using analysis such as DC, AC, and noise, the simulation using transient analysis should be performed to verify the overall performance of the ADC. Since the output of the ADC is in the digital domain, an ideal DAC can be utilized to simply evaluate the ADC output spectrum. The overall performance such as signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), and spurious-free dynamic range (SFDR) can be calculated using the spectrum analysis that utilizes the fast Fourier transform (FFT) analysis.

TABLE I. Coefficient translation

Coefficients	Coefficient values	Passive components
$c1 \cdot k1$	$0.42 \cdot 32M$	$\frac{1}{R_{INT1} \cdot C_{INT1}}$
$c2 \cdot k2 \cdot d2$	$1.09 \cdot 32M$	$\frac{1}{R_{INT2} \cdot C_{INT2}}$
$d1$	2.85	$\frac{C_{FF}}{C_{INT2}}$
$d0$	1.56	$\frac{C_{IFF}}{C_{INT2}}$
$a0$	0.44	$\frac{C_{ELDC,total}}{C_{INT2}}$

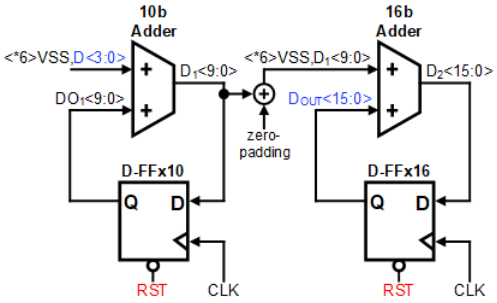


Fig. 5. CoI Filter Implementation.

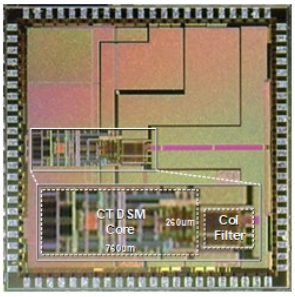


Fig. 6. Chip Photo.

IV. MEASUREMENT RESULTS

The prototype chip was fabricated to verify the operation and performance of the measurement. Fig. 6 shows the chip micrograph of the prototype ADC. The prototype is designed with a 180nm CMOS process. The CT DSM core consists of the 2nd-order loop filter including amplifier and passive RC components, an SAR ADC as the multi-bit quantizer, resistive DAC, capacitive DAC, and digital control logic. The total chip size is 2500 um × 2500 um, including the core, decimation filter, decoupling capacitors, and I/O PADs. The core size of the CT DSM is 760 um × 260 um.

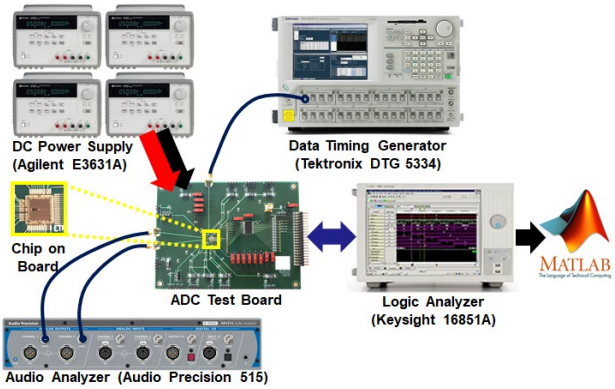
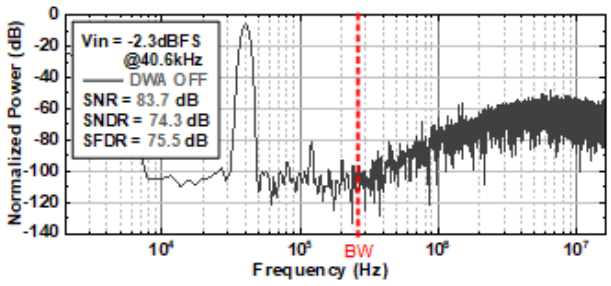
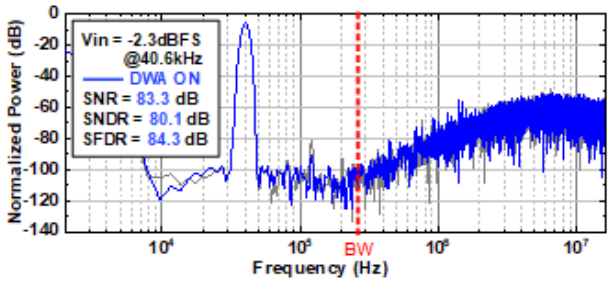


Fig. 7. Measurement Setup



(a)



(b)

Fig. 8. Measurement Result in DSM mode with (a) DWA off and (b) DWA on.

To measure the ADC performance, PCB is designed with the prototype chip on board, and the measurement environment is set up as shown in Fig. 7. DC power supplies are used to provide the power on the chip. For a low-noise input signal source, an audio analyzer (APx515) is used. The data timing generator (Tektronix DTG 5334) is used as the clock source of 32MHz. The output signal of ADC is captured by the logic analyzer (Keysight 16851A) and evaluated using MATLAB.

With a sampling frequency of 32MHz, the proposed CT DSM achieves a bandwidth of 250kHz. Fig. 8 shows the measured FFT spectrum in DSM mode. The 4-bit output from the DSM is directly captured by the logic analyzer for evaluation. The in-band performance is computed by MATLAB using the ideal filter. Without the DWA, the prototype shows a measured SNR of 83.7dB, SNDR of 74.3dB, and SFDR of 75.5dB, with an input of -2.3dBFS at 40.6kHz. With DWA turned on, the prototype shows a measured SNR of 83.3dB, SNDR of 80.1dB, and SFDR of 84.3dB, with the same input conditions. This comparison in

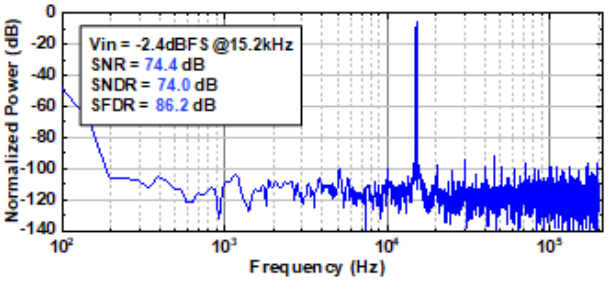


Fig. 9. Measurement Result in incremental mode.

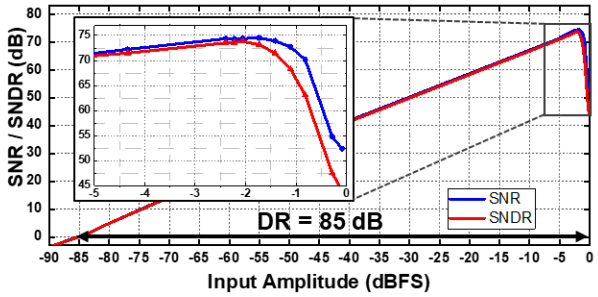


Fig. 10. Measured SNR/SNDR vs. input amplitude in incremental mode.

TABLE II. Performance summary.

Specification [unit]	Proposed Work: DSM / I-DSM mode
Technology [nm]	180
Supply [V]	1.8
Power [mW]	2
F_S [MHz]	32
BW [kHz]	250
OSR	64
SNR [dB]	83.3 / 74.4
SNDR [dB]	80.1 / 74.0
SFDR [dB]	84.3 / 86.2

measurement shows that the DWA improves the harmonics effectively. With a 1.8V supply and power consumption of 2mW, the DSM mode achieves a Schreier Figure of Merit (FoM_S) of 161dB.

The Nyquist conversion rate of the incremental mode in this prototype is 400kS/s due to the clock interface issue. Fig. 9 shows the measured FFT spectrum in incremental mode. The 16-bit output from the CoI filter is directly captured and evaluated. Since the output digital code is already filtered by the designed CoI FIR filter, the output spectrum shows the Nyquist-like noise floor. When the DWA is enabled, the proposed ADC shows a measured SNR of 74.4dB, SNDR of 74.0dB, and SFDR of 86.2dB, with an input of -2.4dBFS at 15.2kHz. Fig. 10 shows the measured dynamic range plot in incremental mode, showing a DR of 85 dB.

The results of the DSM mode and incremental mode show the expected performance, which coincides with MATLAB

simulation, having around a 10dB difference for the measured SNR and SNDR. Table II summarizes the overall specification and measured performance

V. CONCLUSION

The low-noise low-power CT DSM would be a potential solution for a bio-signal acquisition system. As the proposed single ADC also works in a multi-channel environment having low-noise, it would be highly efficient in its energy and area. By implementing this type of ADC using the implantable active device technology, the proposed ADC will be applicable in an implantable medical device and brain-device interfacing.

ACKNOWLEDGMENT

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REFERENCES

[1] S. Wu, Y. Shu, A. Y. Chiou, W. Huang, Z. Chen and H. Hsieh, "9.1 A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s," in IEEE ISSCC Dig. Tech. Papers, Feb. 2020, pp. 154-156.

[2] M. A. Mokhtar, P. Vogelmann, M. Haas and M. Ortmanns, "A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT Incremental Delta–Sigma Modulator With Differentially Reset FIR Feedback," in IEEE Solid-State Circuits Letters, vol. 2, no. 9, pp. 87-90, Sept. 2019.

[3] P. Vogelmann, J. Wagner, M. Haas, and M. Ortmanns, "A dynamic power reduction technique for incremental ΔΣ modulators," IEEE J. Solid-State Circuits, vol. 54, no. 5, pp. 1455–1467, May 2019.

[4] P. Malcovati, SDToolbox 2 [Online]. Available: http://www.mathworks.it/matlabcentral/fileexchange/25811-sdtoolbox-2

[5] J. Wagner, P. Vogelmann and M. Ortmanns, "An Automated Design Environment for CT Incremental Sigma-Delta ADCs," 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, UK, 2020, pp. 1-4.

[6] S. Pavan, R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters, 2nd ed. Pascataway, NJ, USA: IEEE Press, 2017.

[7] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," 2005 IEEE International Symposium on Circuits and Systems, Kobe, Japan, 2005, pp. 184-187 Vol. 1.

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