D-band High Gain and Wide Bandwidth Power Amplifier Design in 65nm CMOS Adopting Dual-Peak G_{max} Technique

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***Abstract* – This paper presents a design of a CMOS D-band high gain and wide bandwidth amplifier adopting the dual-peak G_{max} technique. The proposed amplifier applies the dual-frequency G_{max} technique based on 3-embedding, which provides high gain over a wide bandwidth. By utilizing the degree of freedom of 3-embedding, we designed a core with optimal input and output impedance. After that, a D-band 3-stage power amplifier is constructed using the designed G_{max}-core. When VDD=1V, the measured gain peaks 16.8 dB at 161 GHz with the 3-dB bandwidth of 18.6 GHz and the operating frequency from 150.2 GHz to 168.8 GHz. The maximum output power is 5.65 dBm at 159 GHz and shows performance ranging from 1.39 to 5.65 dBm across the entire operating frequency range. The DC power consumption is 98 mW. The total chip area of the power amplifier is 0.224 mm^2.**

***Keywords*—CMOS, D-band, PA, gain boosting, wideband**

I. INTRODUCTION

In recent years, sub-terahertz systems have been attractive in various applications such as high-speed data communication, spectroscopy, and radar. Among the sub-terahertz frequency bands, the D-band (110-170GHz) is a promising frequency band for 6G communication. Therefore, low-cost and high-density D-band systems using CMOS technology have been extensively studied.

However, the intrinsic gain of transistors is low in the D-band. As shown in Fig. 1, for a 65nm CMOS, a 28um transistor has a G_{ma}/G_{ms} of 6 dB and a unilateral gain (U) of 8 dB. Low intrinsic gain results in increased transistors to implement the high gain amplifier, consuming a lot of power and area.

To solve this problem, the concept of G_{max}, which refers to the theoretical maximum gain of a transistor, was proposed in [1] and implemented through an embedding network. As shown in Fig. 1, a 28um transistor in a 65nm CMOS has a G_{max} of 13.6 dB at 150 GHz, which theoretically allows for implementing an amplifier with a gain per stage that is 5.6 dB higher than U. Subsequently, in [2], a degree of freedom was added to the G_{max}-core design by constructing a 3-component G_{max}-core, which allowed for the free adjustment of input/output impedance for optimized matching. However,

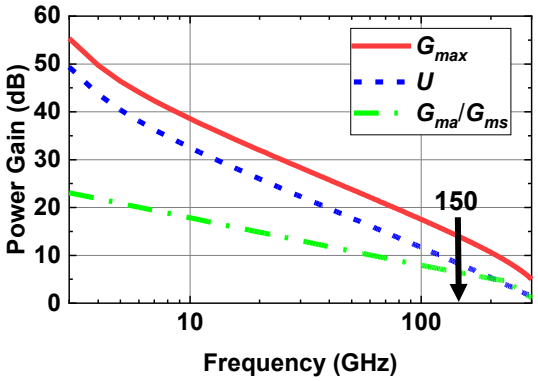

Fig. 1. Simulated gain performances of a 28um transistor for a 65nm CMOS

the G_{max}-core has a narrow bandwidth despite having a high gain. To overcome this limitation, [3] proposed the dual-peak Gmax technology, which can have a wide and high gain in the frequency range between two frequencies where the G_{max} condition is satisfied.

In this article, we demonstrate the design of a high gain and wide bandwidth D-band power amplifier adopting the dual-peak G_{max} technique. Moreover, through load-pull simulation, we found a combination of components among the countless combinations of 3-component elements that can achieve output gain matching and power matching simultaneously at the operating frequency, enabling high gain and high output power simultaneously. Section II describes the design methodology of the Dual-peak G_{max}-core and 3-stage D-band power amplifier. Section III presents the simulation results of the designed power amplifier and concludes in Section IV.

II. DESIGN METHODOLOGY

A. Dual-peak G_{max}-Core with 3-component embedding network

Fig. 2 shows the block diagram of a three-component-based G_{max}-core. By adjusting the values of the three components to satisfy a G_{max} condition [2]:

$$Y_{21,eq}/Y_{12,eq} = -G_{max}, \quad (1)$$

the transistor can achieve a gain equivalent to G_{max}. If (1) is met at only one frequency, it is called a single-peak G_{max}, and if (1) is satisfied at two frequencies simultaneously, it is called a dual-peak G_{max}. As shown in Fig. 3, the dual-peak

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Manuscript Received Mar. 14, 2023, Revised Jun. 12, 2023, Accepted Jun. 19, 2023

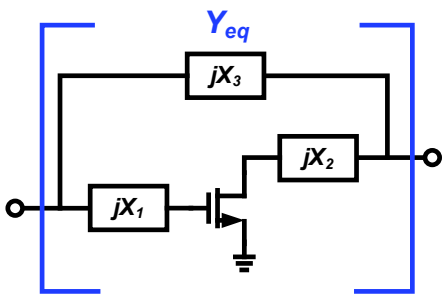


Fig. 2. A block diagram of a 3-component-based G_{max}-core

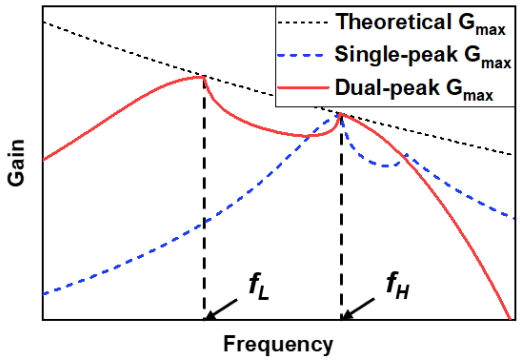


Fig. 3. A comparison of single-peak G_{max} and dual-peak G_{max}

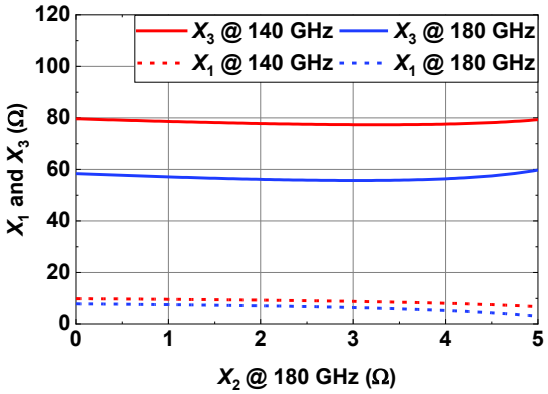
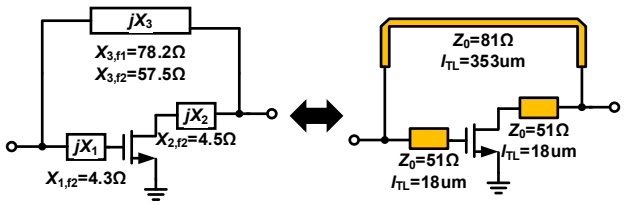


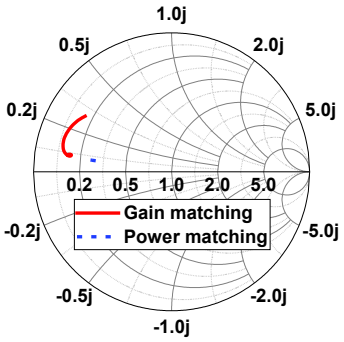
Fig. 4. X_1 and X_3 versus X_2 required to achieve G_{max}-condition with a 28um transistor in 65nm CMOS at 140 and 180GHz

G_{max} has a high gain close to G_{max} over a wide frequency range between the peak frequencies. Therefore, by using a dual-peak G_{max}-core, a broadband amplifier can be easily implemented.

Fig. 4 shows X_1 and X_3 versus X_2 required to achieve G_{max}-condition with a 28um transistor in 65nm CMOS at 140 and 180 GHz. The transistor size is determined considering the gain and output power properties. As shown in Fig. 4, an infinite number of combinations of X_1, X_2, and X_3 can be used to implement the G_{max}-core with three components. However, since the input and output impedance of the G_{max}-core changes depending on the combination, it is common to choose a combination that optimizes input and output impedance matching [2].



(a)



(b)

Fig. 5. (a) Design details of the G_{max}-core that satisfies the G_{max} condition at 140 and 180 GHz and (b) simulated output power and gain matching impedance of designed G_{max}-core from 140 to 180 GHz.

B. 3-stage D-band Dual-peak G_{max}-based Power Amplifier Design

Fig. 5 (a) shows the design details of the core that satisfies the G_{max} condition at 140 and 180 GHz. The values of the three components, X_1, X_2, and X_3, are chosen from the infinite combinations in Fig. 4 to align the output small-signal gain matching and output power matching. In this design, transmission lines (TLs) are used to implement the required reactance values based on the equation [2]:

$$X_{\text{eq}} = Z_0 \sin(\beta l_{TL}) \tag{2}$$

where Z_0 is a characteristic impedance of the transmission line, β and l_{TL} are the beta and length of the transmission line, respectively. X_3, which has a smaller value at high frequencies, can be implemented with a transmission line of a length of lambda/4 or longer [3]. The actual value of the parameters of the TL differs from the calculated value by approximately 5-10% due to losses and couplings in the actual TL. Fig. 5 (b) is the simulated output power and gain matching impedance of the designed G_{max}-core from 140 to 180 GHz. This core chose a combination with a closely located output gain matching and power matching. By designing an amplifier with this proposed G_{max}-core, output power matching can be achieved without small-signal gain degradation. Therefore, achieving a wide, flat, and high gain and output power is accessible.

Fig. 6 shows the circuit schematic of the 3-stage D-band dual-peak G_{max}-based amplifier. G_{max}-core, shown in Fig. 5, constitutes each stage, and the inter-stage matching networks are simultaneously input and output matched over a wide bandwidth using transmission lines. The input and output

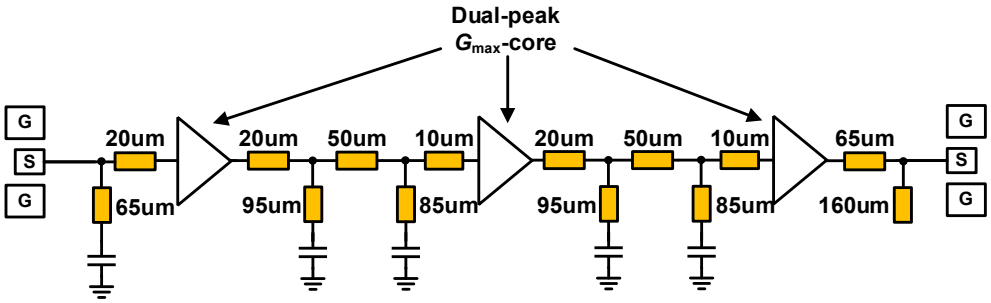


Fig. 6. A circuit schematic of the 3-stage D-band dual-peak G_{max}-based power amplifier

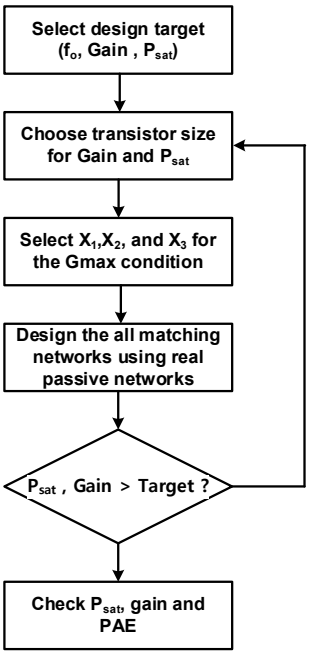


Fig. 7. Design procedure of a dual-peak G_{max}-based power amplifier.

impedance is also broadband matched to 50ohm source and load impedance using transmission lines.

Fig. 7 represents the dual-peak G_{max}-based amplifier design procedure. The optimal transistor size is determined by considering the desired power gain and the output power (or saturated output power, P_{sat}). The X_1, X_2, and X_3 are selected to satisfy the G_{max}-condition at two different frequencies. X_1, X_2, and X_3 are determined from infinite combinations to meet the required objective, e.g., output power and gain simultaneous matching. After selecting the specific X_1, X_2, and X_3 values, implement each with a passive component like a transmission line or cap. The matching networks are also designed with passive components. EM simulation tools such as HFSS or EMX can simulate and verify all passive networks. After the amplifier implementation, check the overall performances, such as power gain, P_{sat}, and power added efficiency (PAE).

III. RESULTS AND DISCUSSIONS

Fig. 8 shows the chip micrograph of the designed 3-stage D-band dual-peak G_{max}-core-based power amplifier. The chip dimensions, including the pads, are 0.77mm x 0.423mm, while the core size without the pad is 0.529mm x 0.423mm.

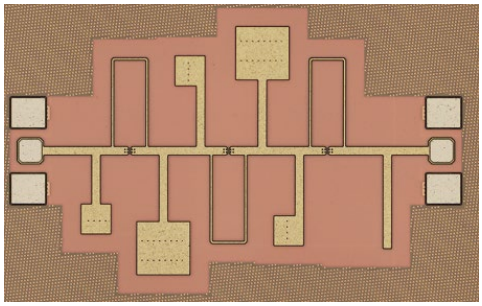
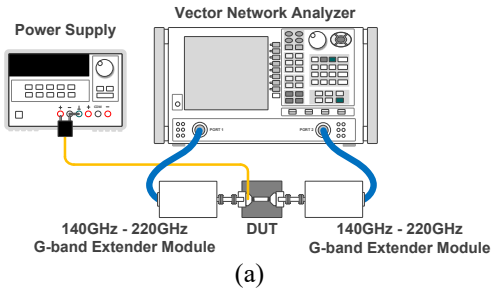
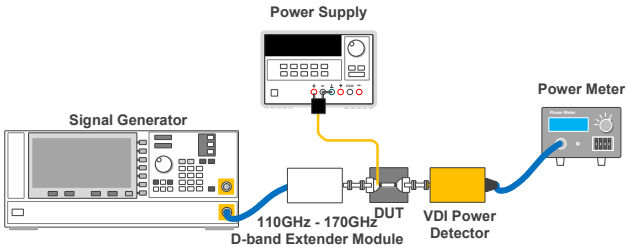


Fig. 8. Chip micrograph of designed 3-stage D-band dual-peak G_{max}-core based power amplifier



(a)



(b)

Fig. 9. Measurement set-ups at G-band. (a) S-parameter measurement and (b) power measurement

This chip is located on a PCB to measure by on-wafer probing. Fig. 9 shows the measurement set-ups at G-band. The S-parameter measurement uses the G-band extension modules (V05VNA2 Series WR05) and a vector network analyzer (N5247A PNA-X). The power measurement uses a signal generator (N5173B) with a D-band extension module (WR6.5SGX) and a power meter (PM5) for the input power source and the output power measurement, respectively. DC bias voltage enters through the input and output probes.

Fig. 10 shows the measurement results with VDD=1V compared to simulation results. The gain peaks 16.8 dB at 161 GHz with the 3-dB bandwidth of 18.6 GHz and the

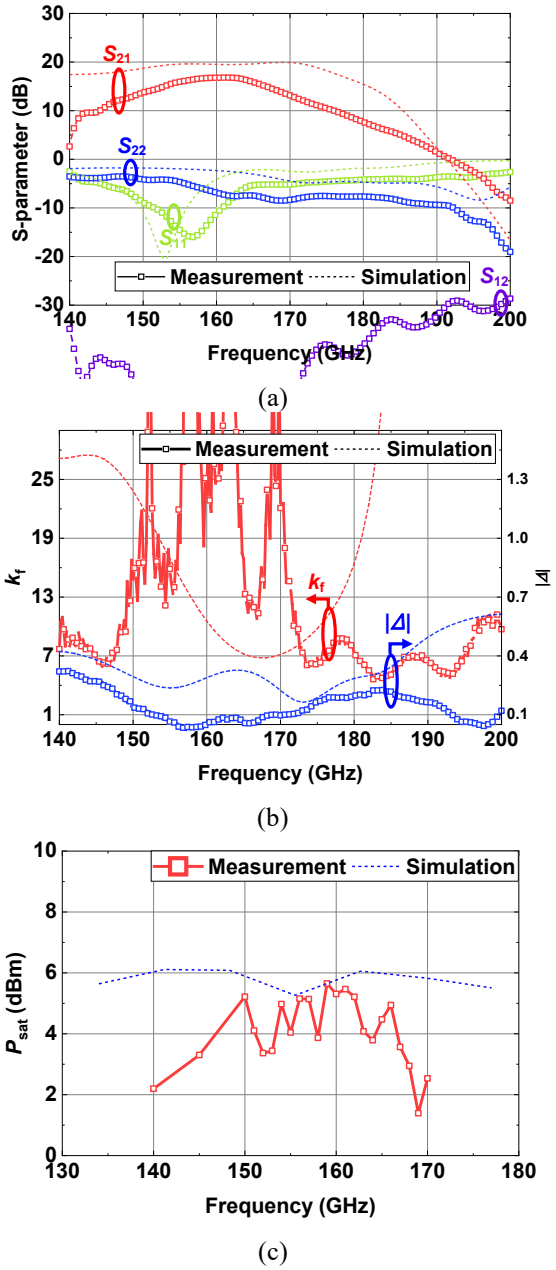


Fig. 10. Measurement results of 3-stage D-band dual-peak G_{max}-based power amplifier: (a) S-parameters, (b) k-factor (k_f), $|\Delta|$, and (c) P_{sat}..

operating frequency from 150.2 GHz to 168.8 GHz. Stability is maintained stable across the entire operating frequency range. The maximum output power is 5.65 dBm at 159 GHz and shows performance ranging from 1.39 to 5.65 dBm across the entire operating frequency range. Compared to the simulation results, the peak gain decreased by 3.1 dB, the bandwidth decreased by 22 GHz, and the maximum output power decreased by 0.46 dBm while dissipating 98 mW PDC. This discrepancy is due to the influence of uncalculated parasitic components caused by inaccuracies in the transistor modeling at high frequencies. The performance is summarized in Table I with a comparison to state-of-the-art. The proposed amplifier achieves state-of-the-art levels of gain, bandwidth, and P_{sat}.

TABLE I. Performance Summary in Comparison with State-Of-The-Art

	This work	**[4]**	**[5]**	**[6]**
Tech.	65nm CMOS	65nm CMOS	45nm CMOS	28nm CMOS
Gain (dB)	16.8	17.5	16	14.3
f_0 (GHz)	159.5	150	141	190
BW_{3dB} (GHz)	18.6	5	31.5	14.4
P_{sat} (dBm)	5.65	10.4	5.4	1.5
P_{DC} (mW)	98	86.3	75	45
Core Area (mm^2)	0.224	0.16	0.072	0.09

IV. CONCLUSION

We proposed a D-band 3-stage power amplifier with high gain and wide bandwidth in this work. A G_{max}-core with a wide operating frequency range of 140-180 GHz is constructed using the dual-peak G_{max} technique. Moreover, the degrees of freedom of the 3-component-based G_{max}-core make the small-signal output gain matching and large-signal output power matching of the *G*max-core close, enabling high gain and high output power simultaneously. By using this G_{max}-core as gain stages, the designed power amplifier achieved a measured peak gain of 16.8 dB and a 3-dB bandwidth of 18.6 GHz with a maximum output power of 5.65 dBm, using DC power of 98 mW when VDD=1V.

ACKNOWLEDGMENT

The chip fabrication was supported by the IC Design Education Center (IDEC), Korea.

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