A Current-mode DC-DC Boost Converter for Automotive LED Headlamp Driver

Woo Jin Hong[1] and Myung Hee Lee[a]
Department of Electrical Engineering, Ulsan National Institute of Science and Technology (UNIST)
E-mail : [1]woojin.hong@unist.ac.kr

***Abstract* - This paper proposes a current-mode DC-DC boost converter for automotive LED headlamp driver. Recently, the trends of an evolution of the LEDs composed by huge pixel, instead of a unit of the LEDs. Therefore, the specifications of DC-DC converters would be much important to operate number of LEDs. In this paper, the current-mode boost converter is proposed to have much wider load current range than the conventional voltage-mode control method. Meanwhile, circuit implementations of building blocks for the proposed boost converter are also presented. The proposed converter has been fabricated through TSMC 0.18-µm 60 V BCD process. The converter operates at a 10 MHz high switching frequency.**

***Keywords*—Automotive LED headlamp driver, Current-mode control, DC-DC boost converter**

I. INTRODUCTION

The technology adopted for the headlights of passenger cars goes beyond simply replacing lighting sources with LEDs from lamps such as bulbs, Xeons, digitizing, ADAS, and fully autonomous using dozens of LED light sources (Pixel structure). The main purpose of this evolution is not just to provide convenience to the driver, but to provide various functions that can be actively adjusted according to the surrounding environment. Fig. 1 shows the expected size of the automotive lighting market from 2016 to 2022. The headlight market accounts for the largest portion of the market each year, and the market size is expected to increase annually to $ 23.6 billion by 2022 [1].

The purpose of adopting headlight technology using dozens of LEDs is basically to adjust LEDs in pixel units, so that high resolution headlights can be realized, and more accurate zone control function can be realized through adaptive functions according to surrounding environment. In addition, it is also possible to implement safety functions such as light source control function and glare-free upward light control when entering the vehicle facing the vehicle.

a. Corresponding author; myunghee.lee@unist.ac.kr

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Fig. 2 shows an LED driver circuit for a headlight consisting of Texas Instruments multiple LED light sources [2]. It shows an example of a matrix LED headlight drive circuit diagram, which basically raises the input voltage through the boost converter, then connects the buck converter in parallel to supply power to each LED. As the number of pixels of the LED increases, the complexity of the drive circuitry that controls each pixel would be increased. Moreover, design of converters that can ensure the power dozens to hundreds of LEDs is essential. Therefore, in this

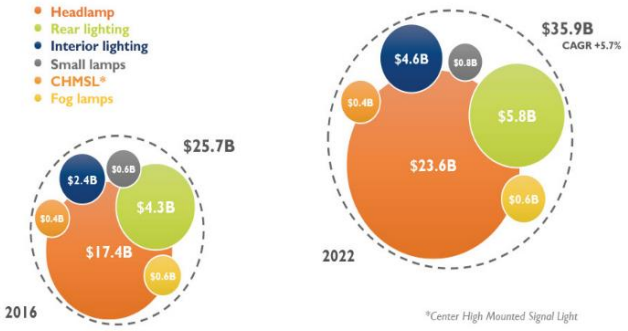


Fig. 1. Automotive lighting market size [1].

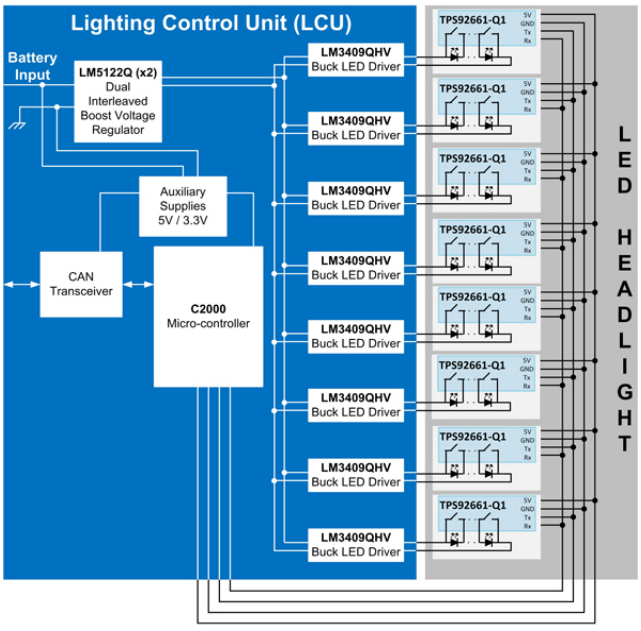


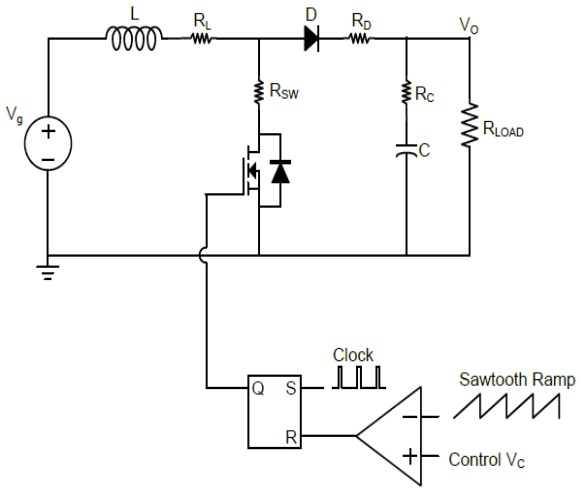
Fig. 2. Lighting control unit for the matrix LED from TI [2].

paper, the design for wide load range current-mode boost converter for LED headlamp driver is proposed.

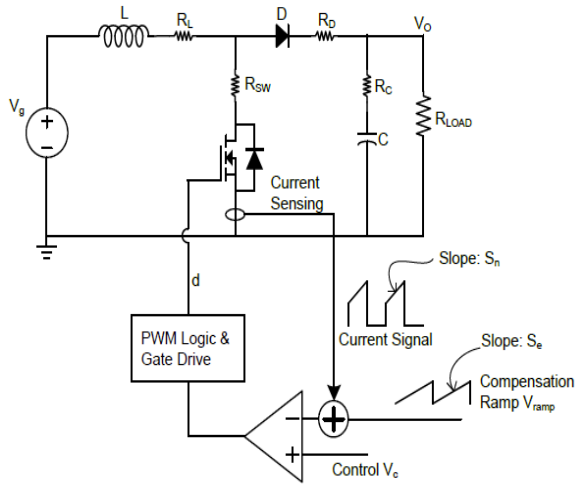
Previous sensing scheme is a digital-based ripple injection current sensor [3]. The inductor current waveform can be emulated while an ADC senses input and output voltages to determine rising and falling slopes of the inductor current. This digital current sensor can achieve the fastest sensing response, which helps to realize the high switching frequency. However, the ADC requires a much faster extra sampling clock than the switching frequency.

In this paper, a 10 MHz current-mode DC-DC boost converter is proposed for the LED headlamp driver. In addition, circuit implementations of building blocks of the DC-DC boost converter such as current sensor, gate driver, and rail-to-rail comparator are presented.

The paper is organized as follows. The comparison of the voltage-mode and current-mode controls is in Section II. The operational concept and circuit implementations of the proposed DC-DC boost converter are introduced in Section III. The experimental results are shown in Section IV. And, Section V concludes the paper.



(a)



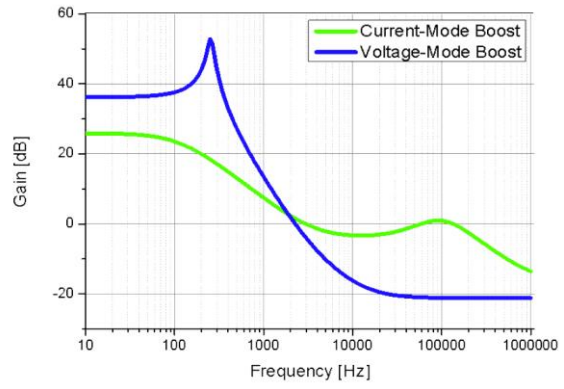
(b)

Fig. 3. Simplified circuit diagrams of (a) voltage-mode boost converter, (b) current-mode boost converter.

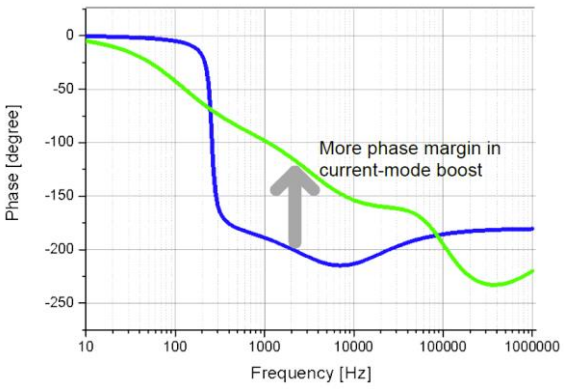
II. COMPARISON OF VOLTAGE AND CURRENT-MODE CONTROLS

Fig. 3(a) and (b) show two different control methods of feedback control, which are voltage-mode and current-mode [4]. The voltage-mode control method generates switching behavior by comparing the output voltage with the triangle waveform to adjust the output voltage. In current-mode control method, the output voltage is adjusted by comparing the current flowing to the switch MOSFET, instead of the triangle wave type. The difference between these two control methods is prominent in ac characteristics, the loop-gain in voltage-mode consists of complex conjugate poles, while that in current-mode consists of single dominant pole. In fact, the dominant-pole in the current-mode is varied depending on the load current. In the boost converter, however, the presence of the RHP zero makes hard to compensate the converter in the voltage-mode, due to additional phase shift about -90 degree. Therefore, the current-mode composed of one dominant pole would be suitable for the boost converter to deal with the loop stability.

Fig. 4(a) and (b) show ac characteristic plots for two control methods [5], [6]. The blue line is the gain-phase plot in voltage-mode, and the green line is the gain-phase plot in current-mode. In voltage-mode control, the gain plot shows that complex poles cause the resonance peaking and subsequently tend to rapidly decrease the gain and phase. Ac characteristics in current-mode can be characterized as one-pole system, thus can achieve higher phase margin than the voltage-mode control. Therefore, in accordance with the design of boost converters, it shows that current-mode



(a)



(b)

Fig. 4. Bode diagrams of (a) voltage-mode boost converter, (b) current-mode boost converter.

control is easier to design and can maintain higher stability with the wide load conditions than the voltage-mode control.

III. CIRCUIT IMPLEMENTATIONS OF THE PROPOSED BOOST CONVERTER

A. Circuit Implementation of Current Sensor

As mentioned earlier, the current-mode control method has the advantage of more stable converter design than the voltage-mode control method. However, as shown in Fig. 3, a current-mode control method requires an additional current sensing circuit that senses the inductor current. Therefore, this paper proposes a peak current sensor that measures the peak current of the power switch NMOS (M_N).

Fig. 5 shows the schematic of the peak current sensor. Basically, it is a structure to measure the current of M_N, and it can indirectly measure the current flowing to M_N by adding M_N' which is a replica switch of power switch NMOS (M_N). a negative feedback loop is implemented to equal the drain voltage of M_N' and M_N, so that the current flows to M_N' as much as size ratio of these two MOSFETs (M_N and M_N'). The sensed current is transmitted to sensing resistor (R_{SEN}) through a current mirror. Finally, the sensed current is converted into the voltage output (V_{SEN}). Therefore, the sensing gain is determined by the product of the ratio of the two NMOS (M_N and M_N') and the sensing resistor (R_{SEN}).

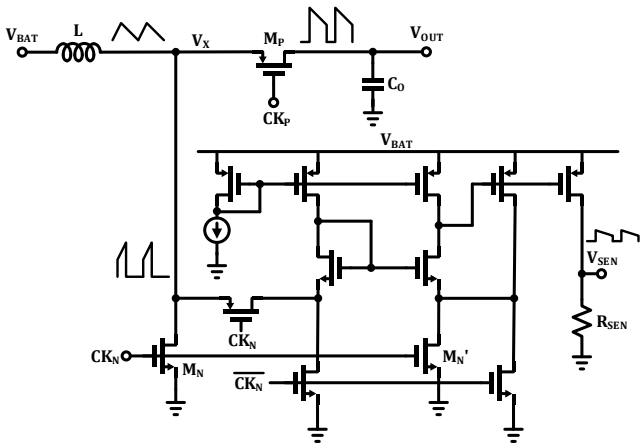


Fig. 5. Circuit implementation of the peak current sensor.

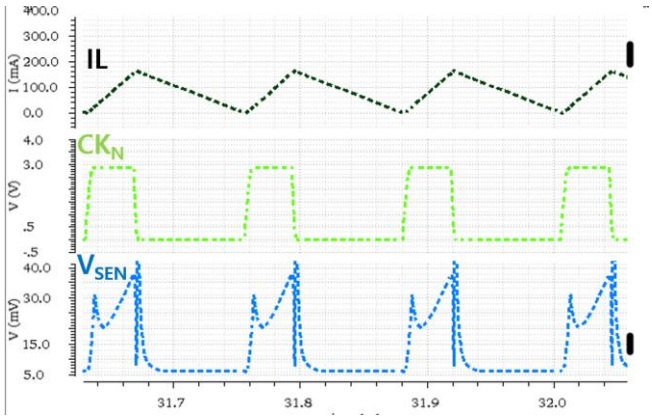


Fig. 6. Simulation waveforms of the peak current sensor.

Since, the CK signal is identical to the PWM signal generated by the converter, the only inductor current generated by the duty on-time can be sensed.

Fig. 6 shows the simulation waveforms of the peak current sensor. It consists of the inductor current (I_L), the NMOS gate signal (CK_N), and the sensing output voltage (V_{SEN}), respectively. Since the peak current of the inductor is sensed, the sensing does not occur when the power switch NMOS (M_N) is turned OFF. When the NMOS is turned ON, we can see that the VSEN also has the maximum value while the inductor current is also at its maximum. The instantaneous peaking at the V_{SEN} right after the power switch NMOS is turned OFF, is just noise during instantaneous switching and can be negligible for converter operations.

B. Gate Driver

Fig. 7 shows the circuit implementation of the gate driver. Since boost converters have two power switches (M_N and M_P), the gate driver is required for switching each power MOSFET. In addition, since each MOSFET is designed with a large size to flow a large inductor current, the inverter chain is implemented to enhance the drivability to the huge input capacitance of power MOSFETs. Also, the inverter chain should be increased to by a factor of four of each size for the size and speed efficiency [7]. Also, two power MOSFETs should not be turned ON at the same time. Otherwise, a short circuit situation will occur in the boost converter, which make the converter have much lower efficiency extremely. Therefore, the gate driver uses a RC-

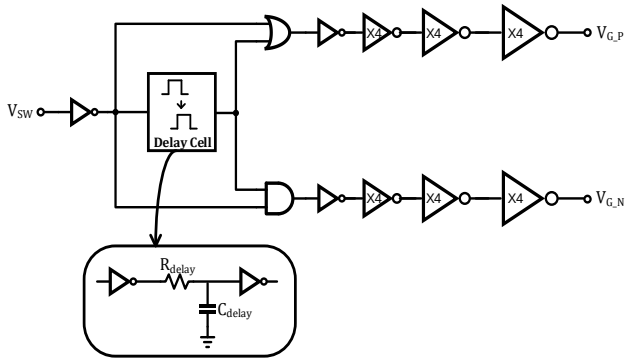


Fig. 7. Circuit implementation of the gate driver.

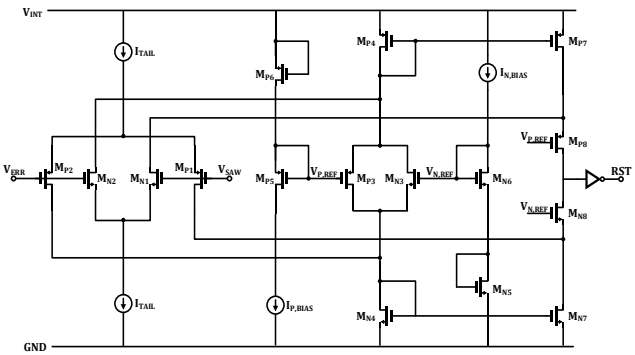


Fig. 8. Circuit implementation of the rail-to-rail comparator.

based delay cell to have a suitable delay when turning ON and OFF two power switches for a nonoverlapping switching behavior.

C. Rail-to-rail Comparator.

Fig. 8 shows the circuit implementation of the rail-to-rail comparator. To generate proper PWM signal, the comparator generates a PWM signal by comparing the current sensing output (V_{SEN}) with the compensator output (V_{ERR}). This proper PWM signal allows the converter to determine the duty cycles and can regulate the output voltage (V_{OUT}). Thus, a rail-to-rail comparator is essential to cover a wide output load current. The basic architecture of the proposed rail-to-rail comparator consists of both PMOS and NMOS input pairs for a wide input voltage range and uses a floating current source to properly bias the current branch (M_{N3} and M_{P3}) [8]. In the output branch, a cascode stage acting as a clamper allows to output the rail-to-rail voltage. In addition, the bandwidth of the comparator is also important since the speed of the comparator also affects the system stability of the boost converter. In this paper, the transition delay of the comparator is designed to be less than 3 ns, which is only 3% of the switching period. Thus, it does not affect the switching behavior of the converter and system stability.

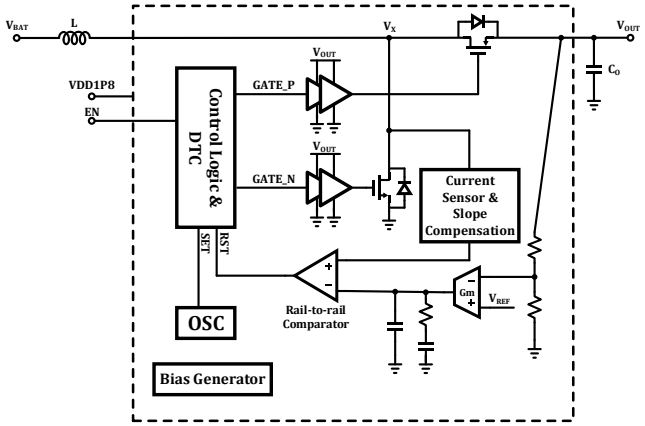


Fig. 9. Top block diagram of the proposed boost converter.

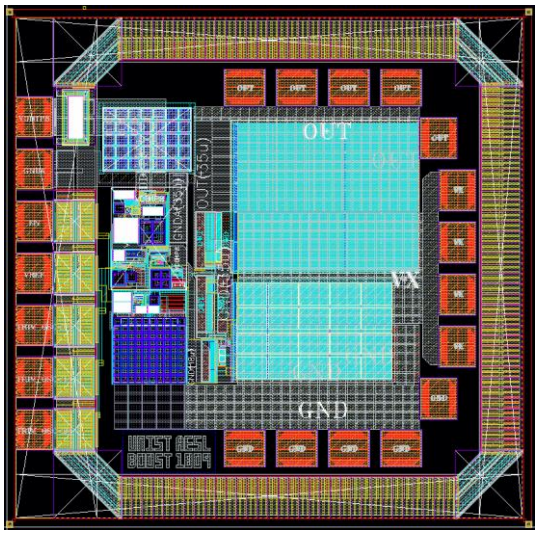


Fig. 10. Chip layout.

D. Top Block Diagram of Proposed Boost Converter.

Fig. 9 shows the top block diagram of the proposed DC-DC boost converter. The building blocks explained earlier are included, which are the current sensor, rail-to-rail comparator, gate driver, and dead-time generator. In addition, a slope compensation is required to operate in current mode control to avoid from a sub-harmonic oscillation [9]-[11].

And a 10 MHz oscillator provides a suitable clock to generate the PWM signal. The band-gap bias generator also provides the power to the building blocks, while providing a reference voltage that regulates the output voltage.

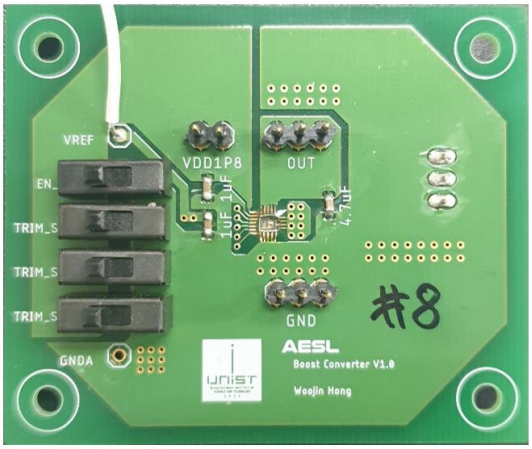
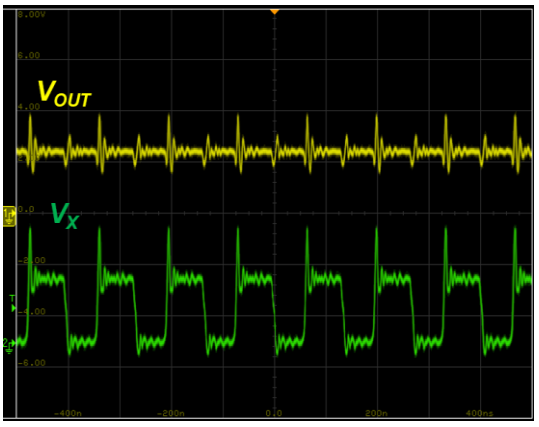


Fig. 11. Test board implementation.



(a)

(b)

Fig. 12. Measured steady-state waveforms under (a) V_{IN} = 2.0 V and V_{OUT} = 3.5 V, (b) V_{IN} = 2.3 V and V_{OUT} = 2.5 V.

Additional enable function can turn ON and OFF the boost converter. The specifications of the proposed boost converter are follows, input voltage from 1.8 to 3.3 V, output voltage from 2.5 to 4.5 V, and maximum allowable load current 0.5A. The LC off-chip components are implemented with 300 nH and 6.6 µF, respectively.

IV. MEASUREMENT RESULTS

The proposed boost converter has been fabricated in a 180-nm CMOS process. Fig. 10 shows a chip layout with a total chip area of 1.01 mm × 1.00 mm including I/O pads and sealing. The off-chip inductor and output capacitor are 300 nH and 6.6 µF, respectively. The output capacitor is composed of three parallel of 2.2 µF to reduce an equivalent series inductance (ESL) of the output capacitor. Otherwise, the output voltage ripple could be degraded in the high switching frequency.

Fig. 11 shows the board implementation. The proposed boost converter is integrated through Chip-on-board (CoB) to reduce the wire bonding resistance and inductance which can affect the switching behavior in the high switching frequency. The off-chip inductor is embedded on the bottom plate to reduce the series resistance which can degrade the conversion efficiency.

The measured steady-state waveforms are shown in Fig. 12(a) and (b) when V_{IN} = 2.0 V, V_{OUT} = 3.5 V and V_{IN} = 2.3 V, V_{OUT} = 2.5 V with R_{LOAD} = 15 Ω.

Fig. 13 shows the measured conversion efficiency as a function of the I_{LOAD} with variations of input and output voltages. The maximum conversion efficiency of 84% is measured under V_{IN} = 1.5 V, V_{OUT} = 2.0 V, and I_{LOAD} = 150 mA.

Table I implies the summary table of the proposed boost converter. The process is adopted by 180-nm BCD process. The specifications of the proposed boost converter are follows, input voltage from 1.8 to 3.3 V, output voltage from 2.5 to 4.5 V, and maximum load current 0.5 A. The LC off-chip components are implemented with 300 nH and 6.6 µF, respectively. Also, the high switching frequency of 10 MHz is adopted, and the maximum efficiency is measured as 84%.

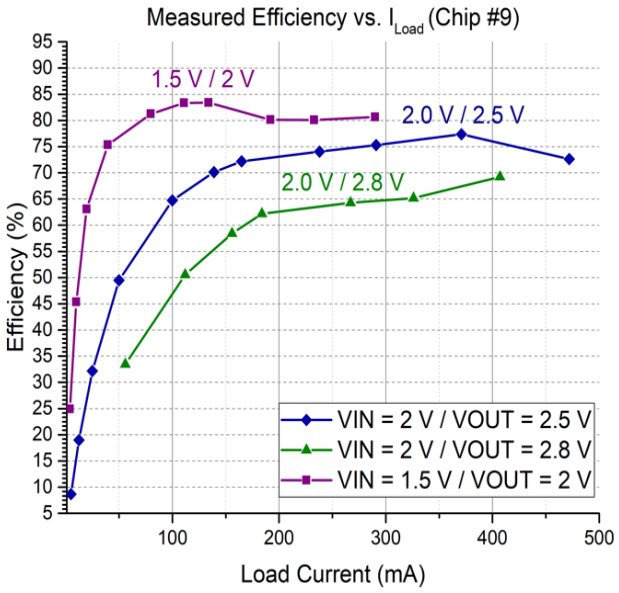


Fig 13. Measured conversion efficiency with respect to the load current.

TABLE I.
Specifications of the Proposed Current-mode DC-DC Boost Converter

Parameter	Value
Process	0.18-µm BCD
Input Voltage	1.8 - 3.3 V
Output Voltage	2.5 – 4.5 V
Inductor (nH)	300
Output Capacitor (µF)	6.6
Max. Load Current	0.5 A
Switching Frequency	10 MHz
Max. Efficiency	84%

V. CONCLUSION

A DC-DC current-mode boost converter design for an LED headlamp has been introduced. In proportion to the larger number of LED headlamps, the performance of the converter must be stable. Compared to the conventional voltage-mode method, the current-mode has more stable ac characteristics, and phase margin. Thus, the current-mode is adopted to enable more stable converter operation. Also, the current-mode converter operation is implemented using the peak current sensor. The building blocks also are introduced to implement the current-mode boost converter. The proposed converter has been fabricated through TSMC 0.18-µm 60 V BCD process. The maximum conversion efficiency is measured as 84%.

ACKNOWLEDGMENT

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Woo Jin Hong was born in Incheon, South Korea, in 1993. He received the B.S. degree in electrical engineering from the Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, in 2016, where he is currently working toward the M.S./Ph.D. combined program. His research interests include analog/mixed-signal integrated circuits, linear/switching power management integrated circuits, and in-vehicle networks for automotive electronics.

Myung Hee Lee received his B.S. in Electronic Engineering from Hanyang University, Seoul, Korea, in 1984, and a M.S. in Electrical Engineering from Arizona State University, Tempe, AZ, in 1990. In 1996, he earned a Ph.D. in Electrical Engineering from Georgia Institute of Technology, Atlanta, GA. He started his industry career as a hardware engineer at Doosan Computer Corp from 1984 to 1988. From 1990 to 1991, he worked at IBM T.J. Watson Lab, Hawthorne, NY, as an engineer before he resumes his Ph.D course. In 1996, he joined Hewlett Packard (later Agilent Technology after the break-up of the company), San Jose, Ca, as a Member of Technical Staff developing IrDA transceiver ICs and Giga-bit fiber-optic transceiver ICs including 4-ch/12-ch parallel optical transceivers. Later he got promoted to an Integrating Manager managing a world-wide R&D organization responsible for various high-speed IC product development. In 2005, he joined Samsung System-LSI division as a VP, Giheung, Korea, managing Display Driver IC (DDI) Development Team. He was responsible for developing various product family such as mobile-DDI, panel-DDI, timing controller, touch sensor controller. From 2012 to 2013, he worked for Hyundai-Autron leading Automotive Semiconductor Development Center managing automotive ECUs (Electronic Control Units) and automotive IC development activities. From 2013, he has served as an Industry-University Collaboration Professor at UNIST (Ulsan National Institute of Science and Technology), Ulsan, Korea. Key area of his research includes automotive ECU architecture, innovative automotive IC architecture and implementations, various high-speed interface and various other mixed-signal IC designs.