A 10 Gbps Optical Receiver Analog Front-End and MZM Driver in 65nm CMOS

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***Abstract* - This paper presents a 10 Gbps optical receiver analog front end and a Mach-Zehnder Modulator (MZM) driver in the 65nm technology. The receiver consists of a Shunt Feedback TIA and a Limiting Amplifier with active feedback for bandwidth enhancement. Offset cancellation is also implemented in the feedback path to minimize random and systematic offsets. The modulator driver adopts a dual-stacked buffer topology with dynamic biasing to generate a high voltage swing. The measured trans-impedance gain of the receiver analog front-end is 74.31 dBΩ with a bandwidth of 16.87 GHz. The DC power consumption is 153 mW (including output buffer) with a supply voltage of 1.8 V. The total chip area of the receiver analog front-end is 0.605 mm^2. The modulator driver achieves a measured voltage swing of 2.02 V_{pp} @ 10 Gbps and a simulated average dynamic power of 230 mW @ 10 Gbps with supply voltages of 1.1 and 2.2 V. The total chip area of the modulator driver is 0.434 mm^2.**

***Keywords*—CMOS, Limiting Amplifier, Optical Modulator Driver, Optical Receiver, Trans-Impedance Amplifier (TIA)**

I. INTRODUCTION

With the rapid growth in bandwidth demand of numerous multi-media applications, silicon photonics is becoming quite an active research area these days [1]-[3]. An optical link has a minimal frequency-dependent loss, low power consumption and can transmit multiple data streams by using multiplexing schemes. Fiber-optic communication has many advantages over electrical interconnects, which are lossy and require very high power for high-speed communication. Therefore, optical transceivers are becoming one of the most promising candidates for high-speed link systems.

The block diagram of a basic optical transceiver is shown in Fig. 1. At the transmitter end, a multiplexer (MUX) is used to serialize the parallel streams of data from multiple channels. A clean-up flip flop, also known as re-timer, is used to remove the jitter and inter-symbol interference (ISI) introduced by the MUX. For proper operation, several clock signals are used to clock the MUX and re-timer, which mandates the use of a Phase-Locked Loop (PLL) for clock generation. A laser diode is a transducer that converts electrical input (current) to an optical signal which is more suitable for long-distance propagation. Generally, for low-speed applications, a trans-conductance amplifier is used to convert the input voltage data to current, which inputs the modulation current directly to a laser diode. For high-speed applications, this direct modulation is not feasible due to a phenomenon known as frequency chirping, which occurs when a laser diode is turned on and off frequently at a high speed. Therefore, for a high-speed optical system, indirect modulation is used in which the laser diode is always on and transmits optical light onto the Mach Zehnder Modulator (MZM). A modulator driver is used to amplify the input data voltage, which modulates the optical signal provided continuously by the laser diode to the MZM.

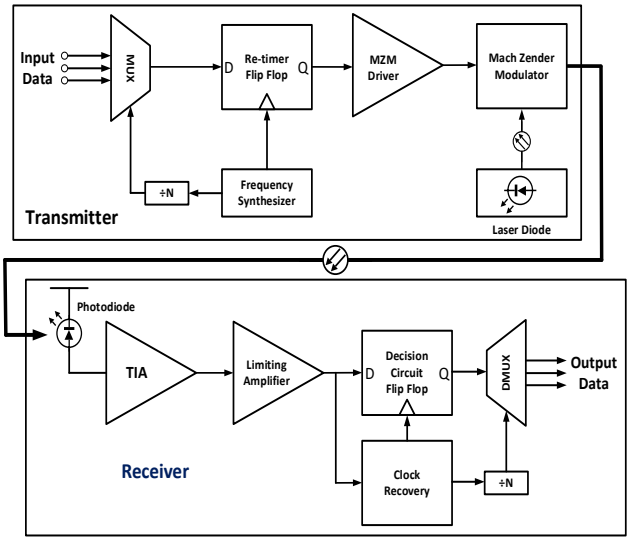

Fig. 1. Block Diagram of Optical Communication System

At the receiver end, a photodiode (PD) is used to convert the optical signal to an electrical one (current) which is input to a trans-impedance amplifier (TIA). TIA is used to convert the input current to a voltage which is further amplified by a limiting amplifier (LA) for detection. A decision circuit flip-flop is used to obtain a cleaner signal by removing the noise of previous blocks. In the end, a de-multiplexer (DMUX) is used to convert the serial data to parallel channels. A clock recovery circuit is used so that the decision circuit samples the high and low levels of data (bits) optimally at the midpoint of each bit for error-free operation [4].

The scope of this work includes the optical receiver analog front-end (OR-AFE) and the modulator driver.

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II. OPTICAL RECEIVER ANALOG FRONT-END

A. Architecture

The overall architecture of the receiver front-end system is shown in Fig. 2. Differential architecture is adopted to minimize the noise and supply parasitics, especially in high-speed circuits. The input to the TIA is single-ended since it is not feasible to use a differential photodiode due to its high input capacitance. So, single-to-differential conversion is employed within the TIA topology by extracting the DC level of the input signal and applying it to the negative terminal of the TIA. The output voltage of the TIA is given to the LA, which acts as a hard limiter for input to the buffer. The buffer is only used for measurement purposes. Since the gain of the LA is very high, even very small mismatches can cause its output to saturate necessitating an offset cancellation block.

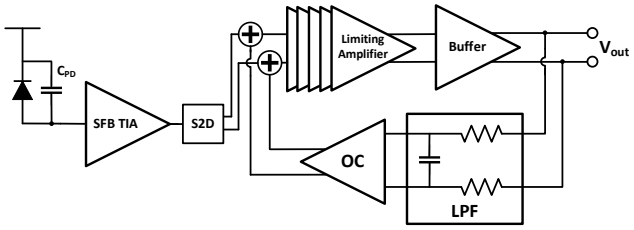
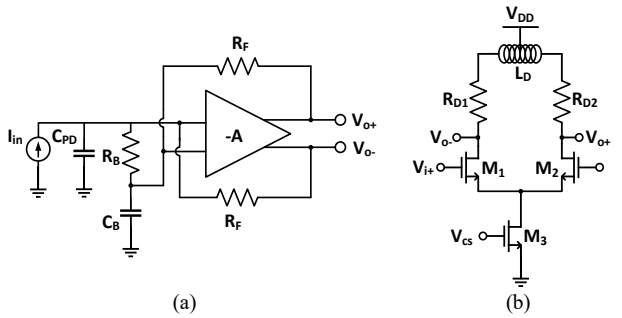


Fig. 2. Optical Receiver Analog Front-End Block Diagram

B. Trans-impedance Amplifier

The design of the TIA is the most crucial part of the receiver as it is the first block and the input-referred noise depends on it, which in turn defines the input sensitivity of the receiver. The performance parameters that dictate the design and choice of TIA topology are gain, bandwidth, noise and linearity/overload response. The main design challenge is that most of these parameters trade off with each other. Hence, choosing the most optimized topology becomes very difficult. The most popular TIA topologies are common-gate TIA (CG TIA), shunt-feedback TIA (SFB TIA) and regulated cascode TIA (RGC TIA). All these topologies have their own benefits and drawbacks [5].



(a) (b)

Fig. 3. (a) SFB TIA Schematic (b) Core Amplifier Single Stage Schematic

SFB TIA was chosen as the topology for implementation as it shows the most optimized trade-offs in terms of the required performance parameters [4]. As the topology employs feedback, it is prone to stability issues that require detailed theoretical analysis for design. Fig. 3(a) shows the circuit schematic of the SFB TIA, which has a differential core amplifier and two feedback resistors. Due to high bandwidth requirement, a 2-stage inductively loaded resistive differential amplifier is employed as the core. The schematic of a single stage of the core is shown in Fig. 3(b).

C. Limiting Amplifier

A limiting amplifier (LA) is used to boost the small amplitude of TIA output voltage to larger levels. LAs usually have a very high gain but should be designed considering the total bandwidth required by the whole system. Due to the high gain requirement, the LA usually employs 3-5 stages. It is very inefficient in terms of area to use inductive peaking to achieve high bandwidth for LA due to a large number of stages.

Hence, our design employs active feedback to boost the bandwidth [6]. A high gain and bandwidth are very difficult to achieve with 1st order gain stages, so 2nd order stages with active feedback are employed to achieve the required performance. A total of 5 stages are used to optimize the gain-bandwidth product of the LA. The block diagram of the 5-stage LA is shown in Fig. 4, where L(s) denotes a single gain cell used in the signal path and $-L_f(s)$ denotes the gain cell in the feedback path. All stages are designed to be the same for symmetry in the layout to avoid mismatches and DC offsets. The input V_{oc} to the 1st stage is provided from the offset cancellation block, as shown in Fig. 2, to further minimize the layout-induced or random offsets. The offset cancellation block takes the differential output signal from the buffer, which is low-pass filtered to extract the DC levels of the output. These output DC levels can have an imbalance between them. Hence, these extracted DC levels are input to a g_m block which acts as a voltage-to-current converter. These balancing currents are fed back to the 1st stage of the LA to compensate for DC offsets.

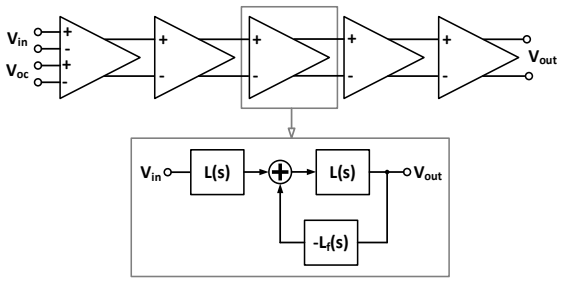


Fig. 4. Block Diagram of Limiting Amplifier

D. Output Buffer

Buffer is used to provide output matching to 50Ω load for measurement purposes [7]. Buffers are power-hungry blocks as they have to provide very high current to output load for achieving sufficient voltage swing. The input transistors in the buffer are designed to be wide to steer high currents. These wide transistors have a serious loading effect on the limiting amplifier degrading the overall bandwidth. The main design challenge in the buffer is to isolate its loading effect on limiting amplifier to avoid bandwidth degradation. A 3-stage inductively loaded buffer with a tapered design

was implemented to alleviate the loading effect. The transistors of 1st stage were designed for minimum loading effect on the LA. The transistors' size and bias currents for the subsequent stages were increased in a tapered manner which alleviates bandwidth degradation while simultaneously providing a high swing to the output load. Fig. 5 shows the schematic and the block diagram of the buffer.

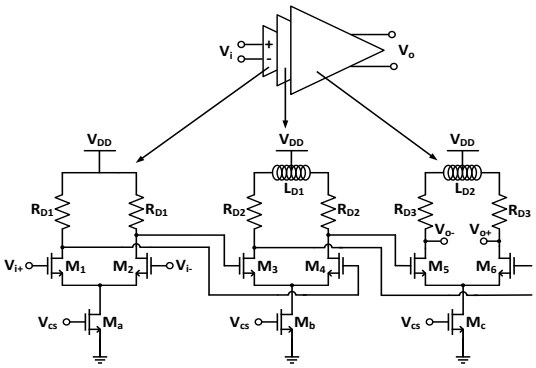


Fig. 5. Output Buffer Schematic

III. MACH-ZEHNDER MODUALTOR DRIVER

A. Block Diagram & Working Principle

The modulator driver is used for modulating the Mach-Zender Modulator (MZM), which receives optical light from the laser diode continuously. The electrical input from the driver modulates the optical output of the MZM. The MZM requires a bias voltage and a very high swing from the driver circuit to operate correctly. Such large swings are difficult to generate due to the low supply voltages of scaled-down silicon technologies. Many circuit-level techniques have been developed for achieving high output swings required for the modulation of MZM [8]. The required swing for our MZM is around 2-2.5 V. In our design, we adopt a dual-stacked buffer topology with dynamic biasing to achieve a high swing of 2.2 V with two supply voltages, VDD1 (1.1 V) and VDD2 (2.2 V). Fig. 6 shows the block diagram of the modulator driver.

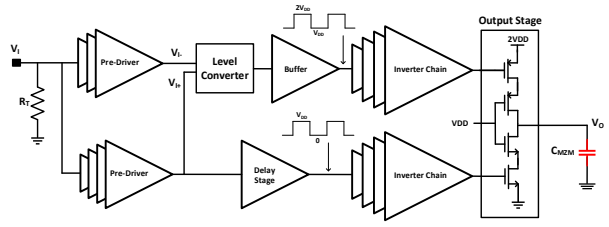


Fig. 6. Block Diagram of Modulator Driver

At the input, a 50Ω resistor R_T is used for input matching. The input voltage is assumed to have an amplitude of at least 500 mV. The pre-drivers fully switch the input voltage between VDD1 and the ground. Pre-drivers are designed using tapered inverter buffers, with one pre-driver having four stages and the other with three stages to ensure complete switching and obtain differential signals. The sizing of both the pre-drivers has been done to compensate for the delays between differential phases due to an unequal number of stages. These buffered signals are input to a level shifter to get two in-phase signals with equal amplitudes but different DC levels, as shown in Fig. 6. A delay stage is added for the signal path between ground and VDD1 to compensate for the delay in the level-shifted signal path. Another set of post-buffer inverter chains with tapered transistor sizing is added to drive the final output stage, which delivers a swing of 2VDD (VDD1 + VDD2) to the load (MZM). The MZM is modeled as a capacitive load of around 300fF, which requires the transistor sizes of the final output stage to be very large. Hence, a 5-stage inverter buffer chain is used before the final output stage to ensure each stage properly drives the next one.

B. Level Shifter

A topology that can ensure high-speed operation up to at least 20 Gbps was required for the level shifter. Capacitive coupled level shifters are generally used for high-speed operation. The topology implemented in our design is known as differentially switched cascoded level shifter [9]. The schematic of the designed level shifter is shown in Fig. 7. The differential inputs are V_{ip} and V_{in} whereas the differential outputs are V_{op_LS} and V_{on_LS}.

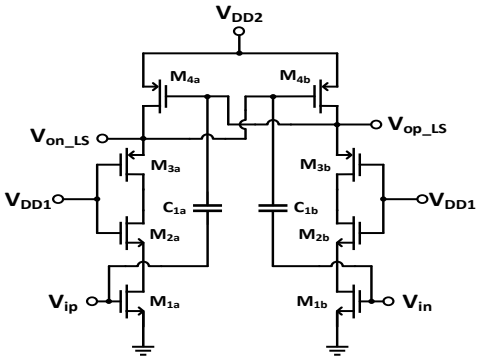


Fig. 7. Level Shifter Schematic

IV. MEASUREMENT RESULTS & DISCUSSION

A. Optical Receiver Analog Front-End

Fig. 8 shows the chip micrograph of the optical receiver analog front-end. The chip area is 0.605 mm^2 with dimensions of 0.864 mm x 0.7 mm. A chip on-board (CoB) setup on a PCB was used to make two sets of measurements (s-parameters and time-domain waveforms) for the OR-AFE.

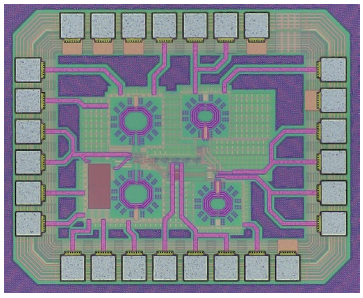


Fig. 8. OR-AFE Chip Micrograph

Rogers 3003 high-frequency substrate was used for PCB production since FR-4 substrate has a high loss at frequencies > 10 GHz. The photodiode was modeled using a capacitor (300fF) on the PCB. Since there is no equipment to provide current as input to the chip, the input impedance of the chip (designed to be 50Ω) was used as a voltage-to-current converter. Fig. 9 shows block diagrams of the required measurement setups.

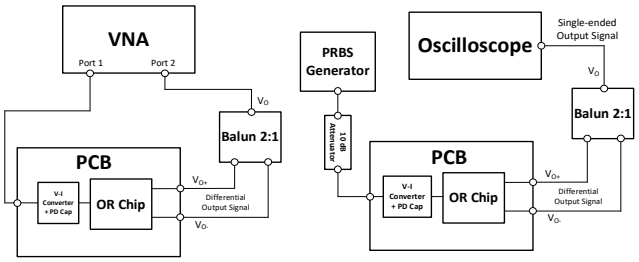


Fig. 9. OR-AFE Measurement Setup for (a) S-parameters (b) Time-domain waveforms

Fig. 10 shows the simulated and measured S_{21} and the trans-impedance gain (G_{TI}) of the whole receiver, which was calculated from S_{11} & S_{21} to de-embed the effect of V-I conversion. The equation that shows this calculation is shown in (1).

$$G_{TI} = 50 \cdot \frac{S_{21}}{1 - S_{11}} \quad (1)$$

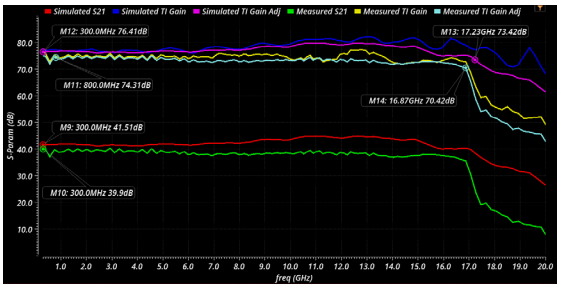
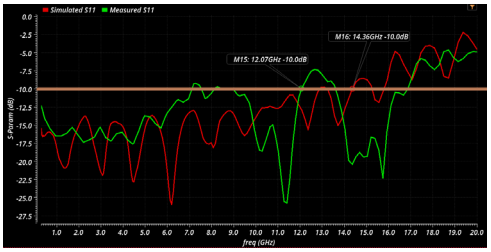
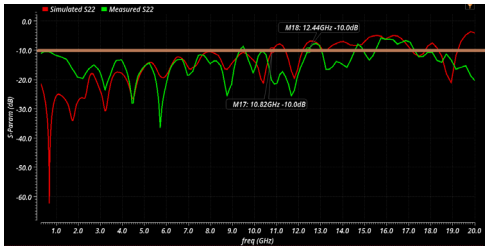


Fig. 10. OR-AFE Simulated & Measured S_{21}, G_{TI} & Adjusted G_{TI}



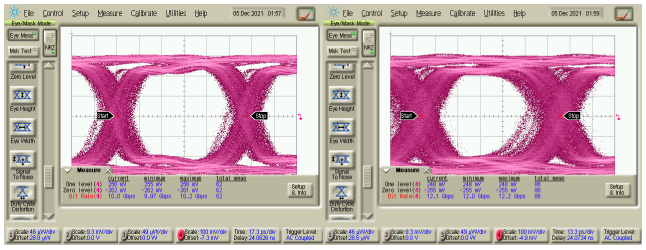
(a)



(b)

Fig. 11. OR-AFE Simulated and Measured (a) S_{11} (b) S_{22}

Fig. 11 shows the simulated and measured S_{11} and S_{22}. We can note in Fig. 10 that there is some ringing or fluctuation in G_{TI} at high frequencies, which results from the degradation of the input matching at high frequencies caused by the wire bond inductances and pad parasitic capacitances. Hence, we calculate an adjusted G_{TI} assuming an ideal S_{11} (-20 dB). It is to be noted that the adjusted G_{TI} is not the actual gain but closely mimics the gain that we would have had if there was no degradation in the input matching. The measured DC gain is around 74.31 dB, whereas the measured 3dB bandwidth is 16.87 GHz. It is to be noted that a higher bandwidth can be achieved when doing measurements with an actual photodiode, as the capacitance used to model the photodiode is a component on the PCB that has a higher impedance roll-off at high frequencies, which degrades the TIA bandwidth. The bandwidth with an actual PD is expected to be 20-21 GHz. Minor differences in the simulated and measured results can be attributed to process variations, inaccuracy of parasitic models, and un-accounted off-chip losses.



(a) (b)

Fig. 12. OR-AFE Measured Eye Diagrams (a) 10 Gbps (b) 12 Gbps

TABLE I. Performance Summary

Parameter	Measured Performance
TI Gain (dBΩ)	74.31
Bandwidth (GHz)	16.87
DC Power (mW)	153
Input Matching S_{11} (dB)	-10 dB @ 12.07 GHz
Output Matching S_{22} (dB)	-10 dB @ 12.44 GHz

Table I gives the performance summary of the whole system. The time domain measurements were done at data rates of 8.5 Gbps, 10 Gbps, and 12 Gbps. The minimum input current to the TIA was limited by the minimum input voltage of the PRBS generator (around 100 mV). Hence, a 10-dB attenuator was used to provide an input current in the range of 500-750μA. The input current amplitude varies at different frequencies due to the imperfect input matching at high frequencies. The measured peak-to-peak amplitudes of the eye diagrams at 8.5 Gbps, 10 Gbps, and 12 Gbps were 0.53 V_{pp}, 0.518 V_{pp}, and 0.503 V_{pp}, respectively. Fig. 12 shows the measured eye diagrams at 10 & 12 Gbps. The equipment limited the measurements at data rates > 12 Gbps as above these data rates, the eye diagrams already deteriorated at the output of the PRBS generator, and the

oscilloscope's sampling rate was inadequate as well. The degradation in input matching due to wire bond inductances and pad parasitics also limit the overall data rate. The system is expected to work with data rates up to at least 10 Gbps if an actual photodiode and a higher-speed oscilloscope were available.

B. Modulator Driver

Fig. 13 shows the chip micrograph of the modulator driver. The chip dimensions are 0.944 mm x 0.46 mm with an area of 0.434 mm^2. A chip on-board (CoB) setup on the PCB was used to make two sets of measurements (s-parameters and time-domain waveforms) for the modulator driver. Since a high output voltage swing of 2.2 V cannot be measured with commercial oscilloscopes, a resistive division network comprising R_1 (450 Ω) and R_2 (50 Ω) is used at the output of the driver on the PCB to reduce the amplitude of output swing for measurement purposes. This resistive network also serves as a matching network for the PCB trace connection at the output. Fig. 14 shows the measurement setups used for characterizing the modulator driver.

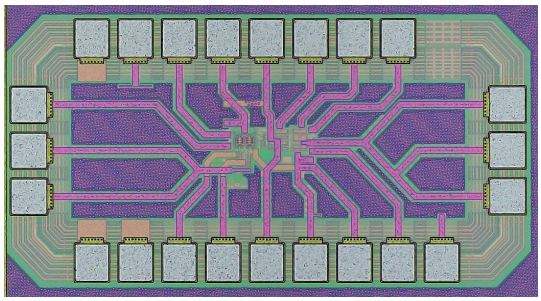
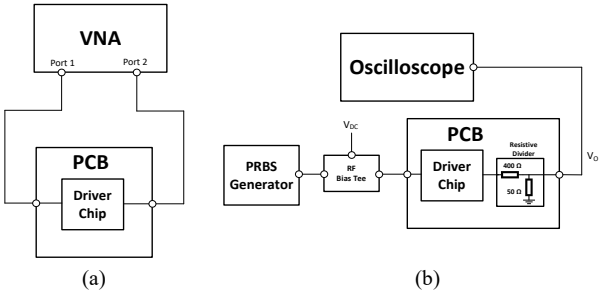


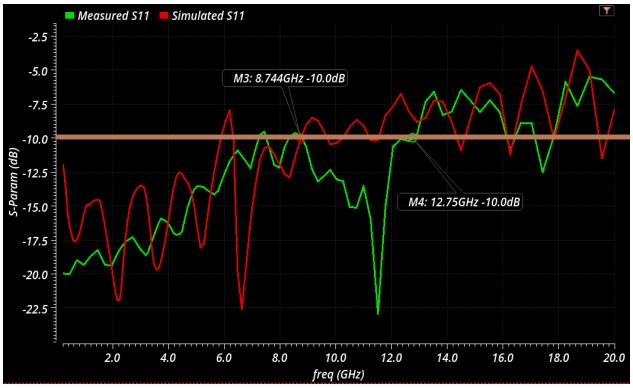
Fig. 13. Chip micrograph of Modulator Driver

For the s-parameter measurements, only the input and output matching (S_{11} and S_{22}) were measured to ensure that the correct signal was applied to the chip. A vector network analyzer (Keysight N5234A) was used for these measurements. For the time domain measurements, a PRBS generator (ML-4009) was used to provide the input signal to the chip via a bias tee. The maximum amplitude available from the PRBS generator was around 400 mV, which was insufficient for switching the on-chip pre-drivers. Hence, an input signal of 400 mV amplitude with a bias level of 550 mV was fed to the chip via a bias tee to ensure correct operation of the circuit.

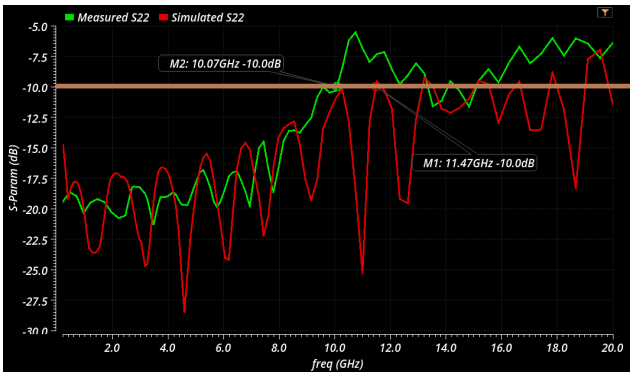


(a) (b)

Fig. 14. Modulator Driver Measurement Setup (a) S-parameters (b) Time-domain waveforms



(a)



(b)

Fig. 15. Modulator Driver Simulated and Measured (a) S_{11} (b) S_{22}

Fig. 15 shows the simulated and measured S_{11} and S_{22} of the modulator driver. In the simulation, we can see the eye diagrams at both the outputs, i.e., before and after resistive division. However, we can only check the eye diagram after resistive division in the measurements. We can extrapolate the actual eye diagram before resistive division from these results. The eye diagrams were tested at data rates of 8.5 Gbps and 10 Gbps. Measurements above these data rates were limited by the measurement equipment, wire-bond inductances, and PCB parasitics, which degraded the input and output matching. Fig. 16 shows the measured eye diagrams at 8.5 Gbps and 10 Gbps. At 8.5 Gbps, the measured amplitude after resistive division is 0.23 V_{pp}, from which we can extrapolate that the amplitude before resistive division will be approximately 2.07 V_{pp}. At 10 Gbps, the measured amplitude after resistive division is 0.224 V_{pp}, from which we can extrapolate that the amplitude before resistive division will be approximately 2.02 V_{pp}.

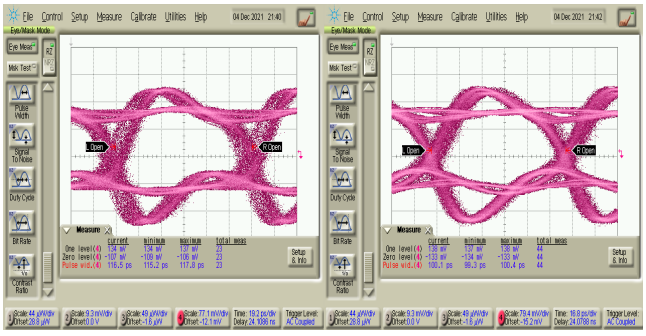


Fig. 16. MZM Driver Measured Eye Diagrams (a) 8.5 Gbps (b) 10 Gbps

IV. CONCLUSION

An optical receiver analog front-end (OR-AFE) and an MZM driver have been designed and fabricated in the 65nm technology. Inductive loading was used for the bandwidth enhancement of the trans-impedance amplifier to achieve high-speed operation, whereas active feedback was employed to boost the gain-bandwidth product of the limiting amplifier to conserve area as it has a large number of stages. A dual-stacked buffer topology with dynamic biasing was used as the MZM driver, which employs a high-speed level shifter to achieve a high-voltage swing. The optical receiver analog front-end achieves a measured gain and bandwidth of 74.31 dB and 16.7 GHz, respectively, whereas the maximum measured data rate was 12 Gbps with an output voltage swing of 0.503 V_{pp}. The MZM driver achieves a maximum a data rate of 10 Gbps with an output voltage swing of 2.02 V_{pp}. The wire bonds, parasitics from PCB and on-chip pads, and the bandwidth of the measurement equipment limit the measured data rate. A data rate of 10 Gbps can be expected if the above-mentioned limitations are removed.

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