Delay Study by Parasitic Capacitance Caused by Inverter Layout

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Abstract - **The propagation time can be obtained by using the rising edge of the CLOCK signal reaching the receiver. To do this, it is necessary to synchronize the start time by synchronizing the impulse generator used in the transmitter and the DTC (Digital-to-Time Converter) part used in the receiver. In the receiver, the reference clock enters the delay line of the DTC. At this time, a template signal is generated by using a signal generated through each delay line. In addition, time information can be obtained by using the signal generated by the impulse generator of the receiver transmitted from the transmitter and whether the template signal is correlated with the correlator. Therefore, the DTC's delay line affects the resolution of time information.**

Therefore, in this paper, we explain the difference and solution of the delay between the simulation in Schematic and the post-layout in the delay line of DTC.

Keywords— **CLOCK, DTC, Time, Delay line**

I. INTRODUCTION

As autonomous cars and IOT (Internet of Things) -based products are popularized, relevant research is actively being conducted, and research on low-power sensors in the wireless environment for collecting various information is attracting attention. Among them, TDC (Time-to-Digital Converter) is widely used as a sensor for measuring the distance of an object [1].

A receiver consisting of an envelope detector and a comparator is used to measure the arrival time of an impulse signal using a time-to-digital converter (TDC). When the impulse signal is received at the receiver, it is amplified via the LNA . Impulse signal enters the envelope detector. The envelope detector generates an envelope of the input signal as an output and determines whether it is higher than the reference voltage in the comparator as shown in Fig. 1 and if it is high, it is determined as the arrival point [2].

Another sensor that can measure the distance of an object is using a correlation-based distance measuring radar. In this case, the sensor takes advantage of the fact that correlation occurs only in two signals with the same frequency characteristics. The sensor uses template signals generated at regular time intervals and shows the degree of overlap of two signals in the integrator only in the form of energy when a signal of the same type as the template signal enters the correlator.

In both cases, the parts of TDC and DTC that are generated at regular intervals are important. At this time, these TDC and DTC are mainly made by arranging several inverters in series. So, we design the inverter on a schematic and run a simulation to check the delay value. However, in this case, it is a simulation result when it has an ideal value. If the post simulation is executed after the layout is performed based on the inverter designed on the schematic, the values are different from the simulation on the existing schematic due to the numerous parasitic components according to the shape of the layout. So, in this paper, we studied how to reduce the difference between the simulation and the post simulation delay using the method of the Lumped C model, which is the fastest and most intuitive, although inaccurate.

II. DESIGN METHODOLOGY

A. DTC

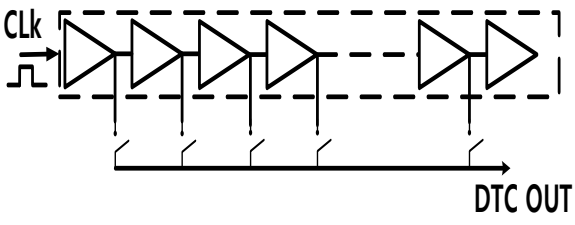

Fig. 1. Delay line schematic

In the structure of the DTC, a constant timing is generated based on a clock signal as follows. 64 delays with the same delay are arranged in series, and each delay output is connected in parallel with a switch and an input of the next delay. The switch is designed so that On / Off is determined by the output value of the binary decoder. When the 6-bit binary code is input to the binary decoder in the FPGA, only

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one output value among the 64 binary decoder outputs has a high value, and the other 63 output values have a low value. In other words, the inverter existing in the Delay line is not affected by the binary value input from the outside, and the delay occurs at the same interval from the input to the output of the Delay line. And only the delay value for the binary value is displayed by the switch installed between the delay blocks. It can pass this output to the Template and Window generators.

B. Parasitic capacitance in the inverter Layout

In the structure of DTC, the delay stage is composed of several inverters. At this time, depending on the layout of the inverter, the delay difference between the simulation on the schematic and the post simulation after the layout may be obvious. In this case, the resolution with respect to time may be degraded, which may result in a significant decrease in the distance resolution of the distance measuring sensor.

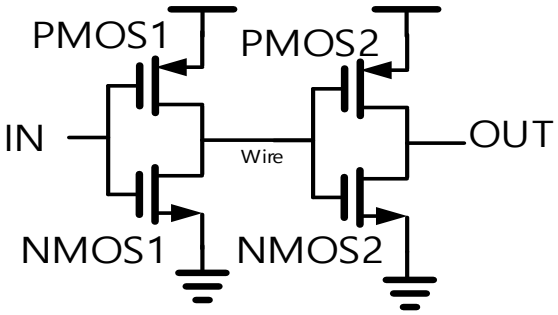
Therefore, we tried to find the best layout by comparing Pre-Simulation and Post Simulation with different layout of inverter.

First, the delay was analyzed before the inverter was laid out. The most fundamental way to calculate delay is to create a differential equation that expresses the output voltage as a function of input voltage and time and then solve it. The solution to this is called a transient response and the delay is the time to reach VDD / 2. This differential equation can be expressed as

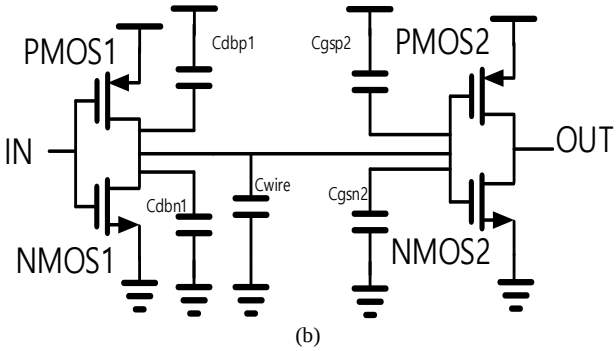
$$I = C\,dV / dt$$

This equation is due to the phenomenon of charging or discharging due to capacitance in a circuit. Since the capacitor cannot change the voltage instantaneously, it takes time for the circuit to switch. Thus, when the capacitor C is charged by the current, I as shown in the above equation, the voltage of the capacitor changes.

Before looking at the transient response in the inverter using the above equation, the structure of the parasitic capacitance in the case of the interconnection between the inverter and the inverter can be expressed as the following figure.



(a)



(b)

Fig. 2. Inverter schematic (a)Inverter structure (b)modeling of inverter

First, the Fig.2. (a) is explained. The inverter located in front is the circuit driving the next inverter located at the end of the wiring. If a voltage rising from 0 to VDD is applied to IN, the delay between VDD / 2 and VDD / 2 is calculated.

At this time, if we check the parasitic capacitance between inverter and inverter, parasitic capacitance exists between Drain and Body of each transistor and parasitic capacitance exists between Source and body.

In the Fig.2. (b), there are other parasitic capacitances except for parasitic capacitance, but only parasitic capacitances between inverters and inverters are important for delay. In the first inverter stage, the parasitic capacitance between the drain and body of the NMOS and PMOS plays an important role in the delay of the inverter. In the second inverter stage, the capacitance between the gate and source of the NMOS and PMOS plays an important role in the delay. In addition, the capacitance at the interconnection part connecting the inverter to the inverter is also involved in the delay.

At this time, the parasitic capacitance between the drain and the body of the PMOS located in the second inverter stage and the parasitic capacitance between the drain and the body of the NMOS were not considered because they are not connected to the node between the inverters. The parasitic capacitance between the source and body of the first stage PMOS, the parasitic capacitance between the source and body of the NMOS, the parasitic capacitance between the source and body of the second stage PMOS, and the parasitic capacitance of the source and body of the NMOS are fixed DC It is not considered because it is connected to voltage.

Before the voltage rises, the input voltage of the first stage is 0, the PMOS of the first stage is ON, the NMOS of the first stage is OFF and the output voltage of the first stage is VDD. At this time, if the voltage rises, the input voltage of the first stage becomes 1, the PMOS of the first stage is turned off, and the NMOS of the first stage is turned on, and the output voltage of the first stage falls to zero.

At this time, as the current is higher or lower than the threshold voltage, it is determined whether to operate in the saturation region or the linear region. So, substituting the equations of the currents in the saturation region and the linear region into the above equations shows whether the current decreases linearly or nonlinearly.[3]

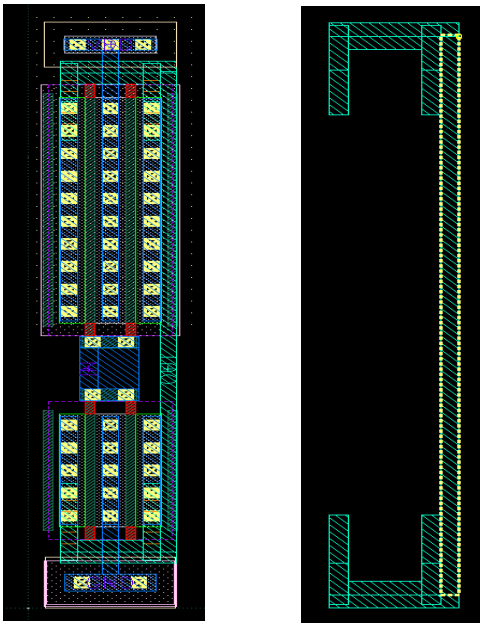
Here, we devised a layout method that considers the capacitance of the first inverter stage except the interconnection and the capacitance of the second inverter

stage by comparing the simulation on the schematic and the post simulation after layout.

III. RESULTS AND DISCUSSIONS

First, an Inverter cell was created. Inveter uses the switching role of NMOS and PMOS, and the inverter presented here has PMOS and VDD lines on the top and NMOS and VSS lines on the bottom. And the ratio of the size of the PMOS and the NMOS is 2: 1. From now on, all layouts have passed the DRC rule of the Foundry Company and all have passed the LVS rule for post simulation. For parasitic RC extraction, we simulated the parasitic resistance and parasitic capacitance by using EDA tool called StarRC.

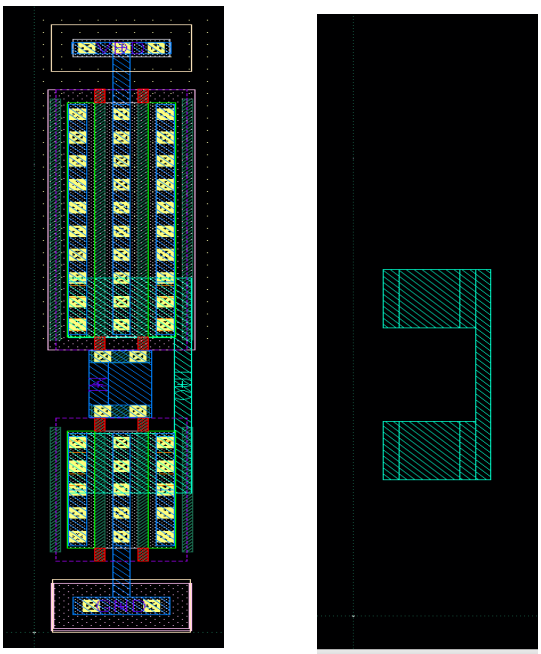
First, prior to comparison, the common part was placed as closest to the distance between NMOS and PMOS as possible to keep the DRC rule as much as possible. In addition, the parts connected to each gate were thickly connected to each other considering the parts to be interconnected later. GND is applied below the NMOS and VDD is applied above the PMOS. In this case, the applied points of the GND and the VDD are applied to all the layout targets to be compared. VDD and GND are also set to be applied to PMOS and NMOS as much as possible.



(a) (b)

Fig. 3. Inverter layout Case1 (a)Inverter layout (b)part of inverter layout

The layout is made as shown in the following figure (a) to have as much capacitance as possible between the Drain part and the body of the first inverter stage. Figure (b) shows only the metal in the drain. This is called Case 1. At this time, the area of the drain metal, which plays an important role in parasitic capacitance, is $0.1515um^2$.



(a) (b)

Fig. 4. Inverter layout Case2 (a)Inverter layout (b)part of inverter layout

This time, the layout is made as follows (a) so that the capacitance between the drain part and the body of the first inverter stage is as small as possible. Figure (b) shows only the metal of this drain part. This is called Case2. . At this time, the area of the drain metal, which plays an important role in parasitic capacitance, is $0.1237um^2$.

At this time, the simulation was described earlier, but one parasitic capacitor was extracted using Parasitic RC Extraction program StarRC without considering the interconnection between the inverter and the inverter. We applied the part and simulated only the parasitic capacitance part in the Drain and Body part of the NMOS and the parasitic capacitance part in the Drain and Body part of the PMOS.

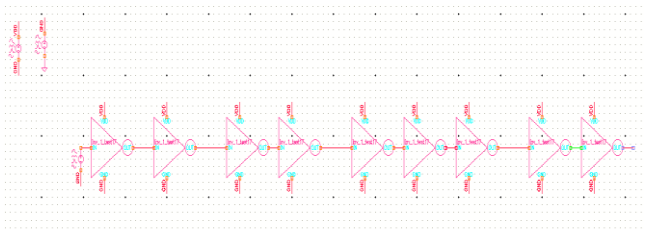


Fig 5. Inverter Layout testbench

As for the method of simulation, several inverter unit cells are arranged in series as shown in the following Fig 5. Also, according to each case, a method of comparing the difference in delay between the input terminal of the inverter arranged at the far right and the input terminal of the inverter arranged at the third from the right was used.

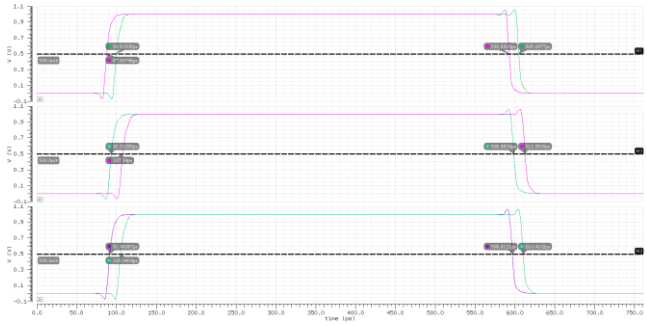


Fig. 6. Inverter simulation

According to the two layout cases, the simulation on the schematic and the post-layout simulation were compared. The first graph above is the Schematic simulation and the second graph is Post simulation according to Case2. The third graph is post simulation according to Case1. The simulation results in Schematic showed a delay of 12.207 ps and the post simulation according to Case 2 showed a delay of 13.592 ps. The post simulation according to Case1 showed a delay of 14.257ps.

Fig. 7. DTC Block layout

In the process of designing the DTC, several delay blocks may be used using the inverter designed above. For example, we have discussed the case where the layout is arranged so that 64 delay blocks are placed in succession. In the Fig. 7 the power lines of VDD and GND enter voltages above and below the delay block, respectively. At this time, depending on the layout method, the direction in which voltage is applied to VDD and GND is different. Then, the voltage values of VDD and GND entering the delay blocks located at the beginning and end may be very different. Therefore, the difference between the delay values of the delays at the beginning and the end may be a factor. In addition, adding 64 delay blocks in series can increase the chip size. So, while designing the DTC, we could reduce the chip size by connecting 32 delays in series as shown in the Fig. 7. above, and then connecting two 32 delay cells in parallel. In addition, the delay blocks are equally supplied with the voltages of VDD and VSS by stacking the VDD and VSS lines as thick as possible and stacking them with multiple metals.[4]

IV. CONCLUSION

The transient response of the parasitic capacitance in the MOSFET is applied to the delay part of the inverter, and the simulation results on the schematic and the post-layout simulation are compared with each other.

As a result, when the capacitance between the drain part and the body of the inverter was reduced as much as possible, the difference between the results of the schematic simulation and the post-simulation after the layout was about 11%. When the capacitance between the drain and the body was made relatively large, the difference between the results of the schematic simulation and the post-simulation was about 16%. Therefore, according to the capacitance between the drain part and the body according to the layout, the difference between the simulation result on the schematic and the post simulation after the layout was about 5%. In addition, it was confirmed that the ratio of the area where the capacitance between the drain and the body occurs and the difference between the delay between the schematic and the layout are 15:12 and 16:11, respectively.

Based on this result, the capacitance between the drain part and the body of the inverter affects the delay.

Therefore, in the case of layout such as DTC or TDC that constitutes a delay line using an inverter, the layout should be considered in consideration of this point. In this way, if the delay value between the schematic simulation and the layout simulation is reduced, the chip can be easily measured when it comes out and the distance sensor can be used to measure the resolution of the distance and the simulation resolution. The difference will be reduced.

REFERENCES

[1] Ahmed Elmallah and Mostafa Gamal Ahmed "A 1.6ps peak-INL 5.3ns range two-step digital-to-time converter in 65nm CMOS" 2018 IEEE Custom Integrated Circuits Conference (CICC). 8-11 April 2018.

[2] Jungwoon Park, and Tae Wook Kim “A Time Domain Artificial Intelligence Radar for Hand Gesture Recognition Using 33-GHz Direct Sampling” 2019 Symposium on VLSI Circuits, 9-14 June 2019

[3] Neil H. E. Weste (2011) CMOS VLSI Design : A Circuit and Systems Perspective

[4] Sungyoung Lee “Correlation-Based High Resolution Long Range Positioning Impulse Radar Design” Seoul : Yonsei University, 2020

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