An Adaptive Power Management IC for Sensor Readout Systems

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***Abstract* - This paper proposes an adaptive wireless power management IC for implantable sensor systems like smart IOL (Intraocular Lens). Depending on the phase, the system operates the sub-circuits with adaptive on/off for low power operation and reducing the noise effect of the inductive link. The adaptive PMIC selectively turns the circuit on/off, which reduces the load power, thereby generating a high DC voltage with a low ac voltage. If power is charged enough, the wireless power transfer (WPT) is cut off and the circuit is driven by internal power. A supply-change circuit and a phase detector automatically change the power supply and phase, respectively. The proposed wireless system can be used for noise-sensitive implantable sensor systems and is built with 180 nm standard process that supports 1.8V/5V transistors. The wireless system operates at a carrier frequency of 13.56MHz.**

***Keywords*—AC-DC converter, Energy backup, Power management, Smart intraocular lens, Wireless power transfer**

I. INTRODUCTION

Real-time monitoring systems using wearable devices can provide information necessary for the diagnosis and treatment of degenerative brain diseases (Alzheimer's and Parkinson's diseases), and a smart lens inserted into the body is a suitable example of monitoring systems that have been studied so far [1]-[3]. A smart lens is an implantable medical device (IMD) with antenna coils wound to suit the appearance of the lens with sensor and detection ICs around them. Bio-signals such as tear glucose [4], eyelid pressure [5], and intraocular pressure [6] are measured with sensors, and data is transmitted externally through the detection IC. The data can be used as information needed to diagnose and treat diseases. These IMDs are implemented in high performance, low power, and ultra-small form through integrated circuit design and require higher performance and efficiency for more precise and effective measurement, analysis, and treatment functions.

Wireless power transfer (WPT) through an inductive link is used in IMD, consisting of an external part, an inductive link, and an implant part. AC signal to a DC signal and the DC voltage is used as an internal circuit supply. The measured bio-signal can be transmitted from the implant part to the external part in the same way as load shift keying (LSK). In implementing a monitoring system with a smart lens using an inductive link type wireless power technique, low wireless power is transmitted due to coil limitations in the smart lens structure, and conventional IMD always operates and uses power, which consumes a lot of power [7]-[9]. In addition, existing studies measure bio-signals while power is being supplied, but there is a noise effect due to the inductive link [10], [11]. In the wireless power technique using an inductive link, coupling variation may occur depending on factors such as coil angle, distance, etc. This can affect the input voltage, load, and internal node. It also reduces power efficiency. To improve these, a method to determine whether to amplify 2x/3x after monitoring the V_{IN} was introduced [12]. However, the additional circuit for V_{IN} monitoring acts as load power, which is a burden to store high internal power at low received power, so load power must be minimized during power storage. Reliable data is required for accurate diagnosis and monitoring, and if the bio-signal can be measured with the WPT removed, noise effects caused by the inductive link can be eliminated.

This paper proposes adaptive power management so that it can store power even in low receiving power and drive internal circuits while stopping WPT. Chapter II will describe the adaptive power management system and the system behavior according to the phase, and the detailed description of the sub-circuit is the external part is a transmitter that uses a power amplifier to run the primary coil (L_1). When the primary coil is operated, the secondary coil (L_2) is induced by the Faraday law and the AC signal is transmitted to the implant part by LC resonance. The rectifier converts are covered in Chapter III. Chapter IV will describe the measurement results, followed by a conclusion in Chapter V.

II. SYSTEM ARCHITECTURE

Fig. 1 (a) shows the proposed adaptive power management system and adaptive operation for each phase, and each sub-block operates according to steps. First, from Fig. 1 (b), which shows phase 1 (start-up), the AC voltage transmitted through the inductive link is converted to DC voltage (V_{REC}) through a voltage multiplier and V_{REC} is used as a digital circuit power supply. If excessive WPT occurs, the voltage of V_{REC} may exceed the operating range. To prevent this, over-voltage protection (OVP) is added to V_{REC} node. After that, when a non-overlapping clock is generated in the clock generator, it becomes phase 2 named power charging (Fig. 1 (c)). The non-overlapping clock is applied to the power gate driver along with the CTRL1 signal generated by the phase detector. The power gate driver is a circuit that drives a step-up DC-DC converter with a switched-capacitor structure according to the phase, and the SC energy booster

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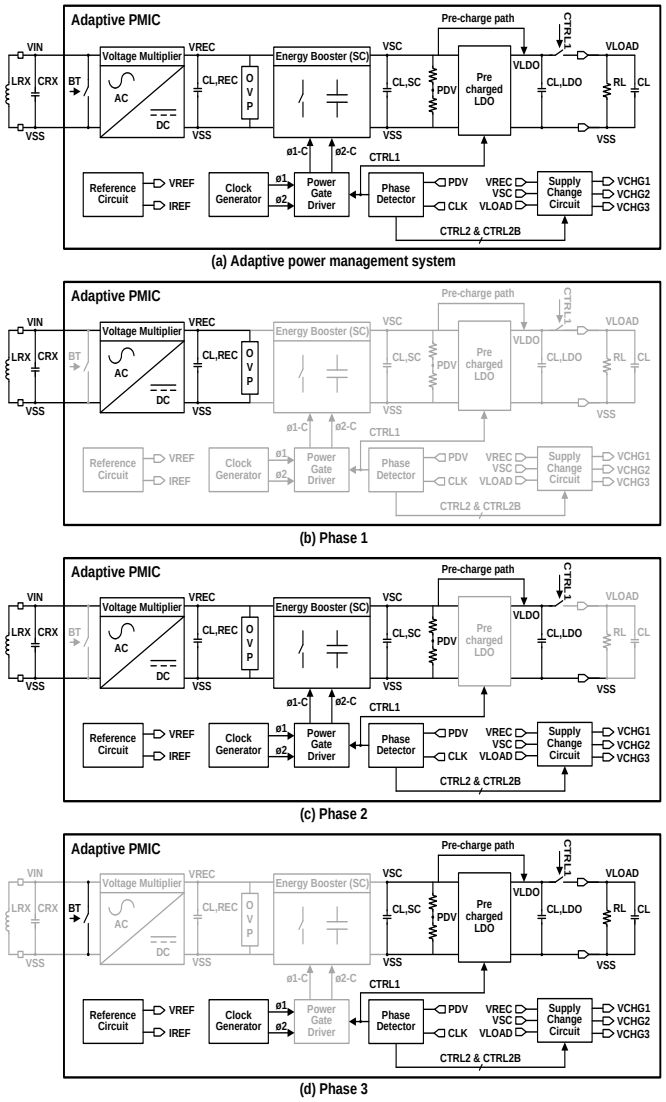


Fig. 1. Proposed adaptive power management system: (a) overall structure, (b) phase 1, (c) phase 2, (d) phase 3.

is operated in phase 2. The SC energy booster generates high DC voltage (V_{SC}) from low DC voltage (V_{REC}) and DC-DC conversion was adopted after AC-DC conversion to improve overall system efficiency.

During phase 2, the voltage (V_{LDO}) of the LDO is also pre-charged through the pre-charge path to increase the operating time. When the internal circuit operates after removing the WPT, the reference circuit produces V_{REF} and I_{REF} used by phase detector, LDO, and clock generator. The phase detector compares V_{SC} voltage divided values of P_{DV} and V_{REF} to determine phase. When V_{SC} increases and $P_{DV} > V_{REF}$, it become to phase 3 named sensing (Fig. 1 (d)) and the WPT is cut off. The LDO generates a constant V_{LOAD} using the stored V_{SC} and it used as an internal circuit power supply. Supply change circuit is a circuit that automatically changes the supply required for each circuit according to the phase, allowing each circuit to operate when WPT is off. Adaptive power management can reduce load power per phase by selectively operating the circuit according to the phase, making it possible to store high power even in weak WPT, and to drive the internal circuit after removing WPT. It can eliminate the inductive noise effect on the internal circuit.

III. BUILDING BLOCK DESIGNS

A. Voltage Multiplier

Due to the structural limitations of the smart lens, weak AC voltage is transmitted through the inductive link, and a constant DC voltage can be used to drive the circuit. As shown in Fig. 2 (a), three voltage doubler structures are connected in series to boost the voltage, and each diode uses a low-V_{TH} PMOS to reduce the diode voltage drop according to V_{TH}. In addition, to eliminate the increase in V_{TH} due to the body effect, two identical PMOS were used to perform dynamic body biasing so that the PMOS body became the higher voltage among the anode and cathode. Instead of passive-type PMOS, an active voltage doubler using a comparator or V_{TH} reduced diode can also be used [13], [14]. However, a passive type PMOS diode was used due to the need for high AC input, increased load power due to the comparator, and insufficient V_{TH} to reduce the effect.

B. SC Energy Booster

Fig. 2 (b) shows the SC energy booster. Three conventional switched capacitor converters were connected in series to create a DC voltage up to 8 times larger than the input DC voltage. The gate voltage and the supply voltage of the transmission gate switch (TG) must be increased together with the V_{SC} voltage increase so that the TG can be turned on/off properly and a high V_{SC} can be made. To this end, the peak voltage of the non-overlapping clock was made equal to V_{SC}, and a supply.

C. Pre-charged LDO

As shown in Fig. 3, a pre-charged LDO is an LDO that adds a pre-charge path to a conventional LDO. During phases 1 and 2, CTRL1 has a low value, SW1 is turned on, the path transistor is turned off, and MUX is connected to V_{SS}, so SW2 is turned off. In addition, TG1 and TG2 are turned off and the gate voltage of the path transistor and V_{LDO} are not discharged. The error amp's supply is the V_{OP} which is the output of the MUX. Since the initial V_{OP} value is V_{SS}, the error amp does not work, reducing power consumption between phases 1 and 2. The pre-charge path operates in phase 2 where the V_{SC} increases, with six PMOS diodes connected to the series and the V_{LDO} is pre-charged through

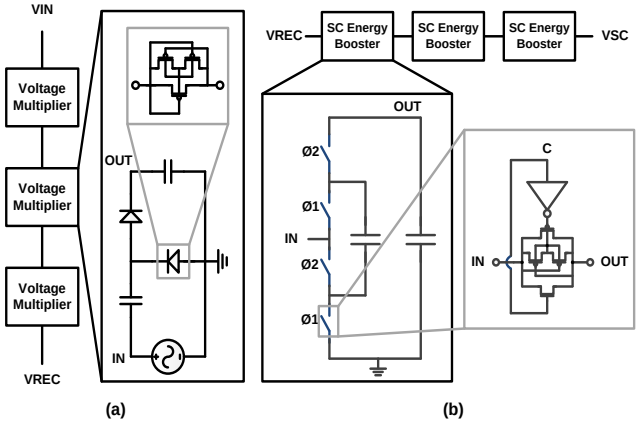


Fig. 2. Block diagrams of the (a) voltage multiplier and (b) SC energy booster.

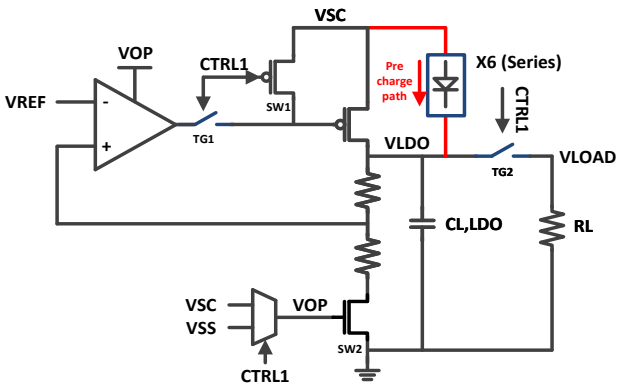


Fig. 3. Block diagram of the pre-charged LDO with load.

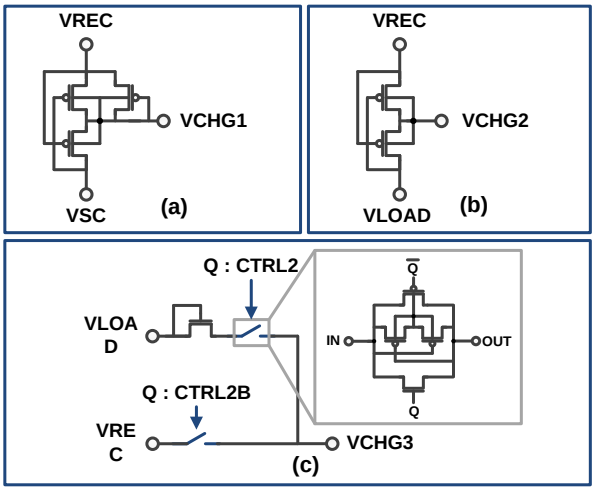
that path. For example, if the V_{SC} is 4.8V and the PMOS transistor's V_{TH} is 600mV, then the V_{LDO} is 1.2V. During phase 3 operation, $C_{L,LDO}$ is charged through the path transistor in V_{SC}, and if V_{LDO} is pre-charged, it is possible to create a supply voltage using less power than charging V_{LDO} at 0V. Simply put, making a V_{LDO} 1.2 to 1.8V requires less power than making a 0V to 1.8V, so it can also operate for longer periods at V_{SC}. The pre-charge function allows the circuit to be driven for longer when charging.

D. Supply Change Circuit

A supply change circuit is a circuit that changes the supply inside the circuit according to the phase. As shown in Fig. 4 (a)-(c), it is composed of three sub-blocks. Fig. 4 (a)-(c) indicate V_{CHG1}, V_{CHG2}, and V_{CHG3} respectively, which automatically changes the higher voltage among V_{REC}, V_{SC}, and V_{LOAD}. Unlike Fig. 4 (b), Fig. 4 (a) has one more PMOS diode, which is added to provide power through the diode even if the two PMOS on the left side are off when the voltage of V_{REC} and V_{SC} is similar and the power is not supplied to V_{CHG1}. Fig. 4 (b) provides power to the phase detector through V_{REC} during phases 1 and 2, and power from the V_{LOAD} generated by the LDO in phase 3. Similar to Fig. 4 (b), Fig. 4 (c) also supplies V_{REC} and V_{LOAD} voltages depending on the phase, but there is a difference in supplying to the reference circuit and clock generator after dropping by NMOS diode voltage. Diode voltage drop is applied to V_{CHG3} to generate a low-frequency clock and align V_{CHG3} to the supply range of the reference circuit. The supply change circuit takes a passive structure to eliminate unnecessary power consumption between supply changes and to operate stably. Fig. 4 (d) shows the supply information for each circuit.

E. Phase Detector

The phase detector is a circuit that distinguishes the phase, consisting of a strong-arm capacitor, D-flip flop, 2-1 MUX, and level shifter, as shown in Fig. 5 The voltage divided value of the V_{SC}, P_{DV}, is compared with V_{REF} as input, and if it is $V_{REF} > P_{DV}$, the current circuit is phase 1 and 2, and if the P_{DV} is higher than V_{REF}, it becomes phase 3. The strong-arm comparator compares P_{DV} and V_{REF} for every clock and maintains the detection result by using the SR latch attached to the output of the comparator. Initially, the Q_{LATCH} of the



Supply	Supply Composition	Using Supply
V_{CHG1}	V_{SC}, V_{REC}	EB, PGD, CG, PD
V_{CHG2}	V_{LOAD}, V_{REC}	PD
V_{CHG3}	V_{LOAD}, V_{REC}	RC, CG

(d)

Fig. 4. Block diagram of the supply-change circuit (a) V_{CHG1}, (b) V_{CHG2}, (c) V_{CHG3}, and (d) summary table

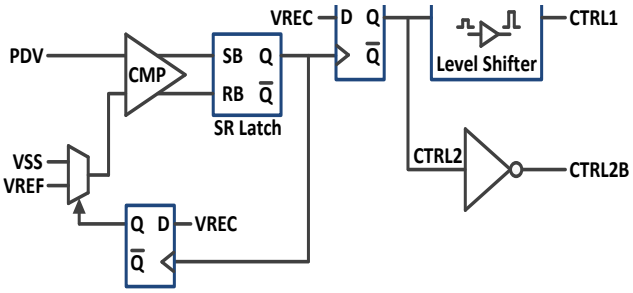


Fig. 5. Block diagram of a phase detector.

SR latch has a low value. When $P_{DV} > V_{REF}$, the Q_{LATCH} goes high and a positive edge occurs. This acts as the clock of the D-flip-flop. Unlike the CTRL signals in phases 1 and 2, the CTRL signal is inverted and the signal of MUX is changed from V_{REF} to V_{SS} to keep phase 3 even when P_{DV} decreases, thereby making the CTRL signal constant. Level shifter shifts CTRL2 signal to make CTRL1, which is used where a high CTRL signal is needed as V_{SC} increases. For the stable phase detecting operation, the voltage of the internal node must be initialized. By applying V_{REF} to the RESETB part of D-flip-flop using the point that V_{REF} is created after V_{REC} generation, the internal voltage can be initialized before the phase detector operation.

Fig. 6 shows the clock generator configuration, which generates frequency with the current-starved oscillator and connects D-flip-flop to series to divide frequency. Thereafter, a high voltage clock is generated through a level shifter, and two non-overlapping clocks are generated by a non-overlapping clock generator. The clock is used for a DC-DC converter, and as the V_{SC} increases, the gate voltage of the transmission gate must also increase to produce a high DC voltage. Therefore, a clock with an increased peak value is required.

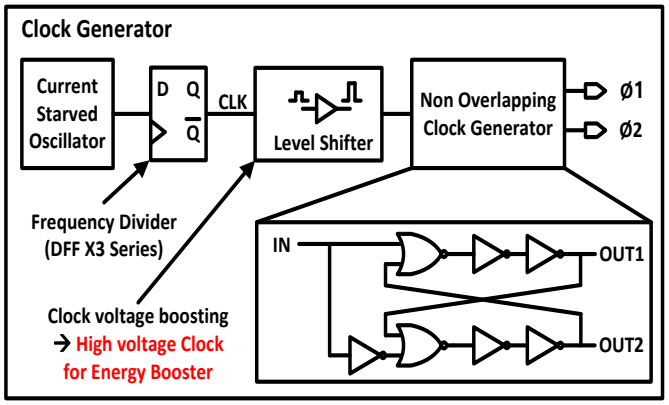


Fig. 6. Block diagram of the clock generator

IV. SIMULATION & MEASUREMENT

A. Transient Response

Fig. 7 shows the simulation results according to the transient. Fig. 7 (a) shows the main operation, (b) shows the control signal, and (c) shows the supply change voltage. Phase 1-4 shows the phase classification according to transient. In phase 1, V_{REC} is generated through the inductive link and supplied to the digital circuit and reference circuit to generate the clock and V & I reference. When the clock is generated, the SC energy booster operates and the V_{SC} increases as in phase 2, and the V_{LDO} value increases as the LDO is pre-charged through the pre-charge path. As shown in Fig. 8 (c), the two PMOS on the left in Fig. 7 (a) are turned off in a similar interval between V_{REC} and V_{SC}. In this case, it is not possible to supply to each circuit, but an additional diode path makes it possible. Because it is a diode path, the value of V_{CHG1} is reduced to V_{REC} - $V_{TH,diode}$, but it maintains the value of V_{CHG1} in that section.

When the V_{SC} increases and becomes P_{DV} > V_{REF}, the CTRL signal in the phase detector, as shown in Fig. 7 (b), is reversed and moved to phase 3. The CTRL1 signal is used where high voltage control is required according to the V_{SC}, so the CTRL1 signal is the same as the $V_{SC,}$ and the CTRL2 signal is equal to V_{LOAD}. In phase 3, WPT is cut off and the internal circuit is driven with the generated internal power. There is a difference between V_{CHG2} and V_{CHG3} in this phase. Since V_{CHG3} is a supply to the reference circuit and clock generator, it is supplied after the diode voltage drop to make it similar to the supply voltage and frequency in phases 1 and 2. Therefore, voltage difference occurs as much as $V_{TH,diode}$. Since the V_{REF} value becomes 0V before V_{CHG3}, the D-flip-flop of the phase detector is automatically reset and operates as phase 2.

B. Power Efficiency

Fig. 8 shows the efficiency of the voltage multiplier and SC energy booster. The effect of $V_{TH,diode}$ drop is relatively different according to the V_{IND} value. If the V_{IND} is low, the efficiency of the voltage multiplier decreases because the relative voltage drop is increased, and the low voltage is stored. In the case of SC energy booster, since the conversion ratio is 8X, the higher the V_{REC}, the lower the efficiency.

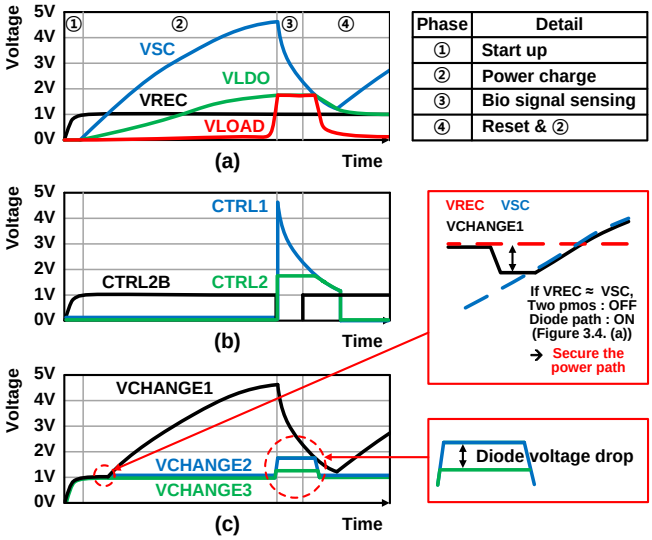


Fig. 7. Transient waveforms: (a) main operation, (b) control signal, (c) supply change voltage.

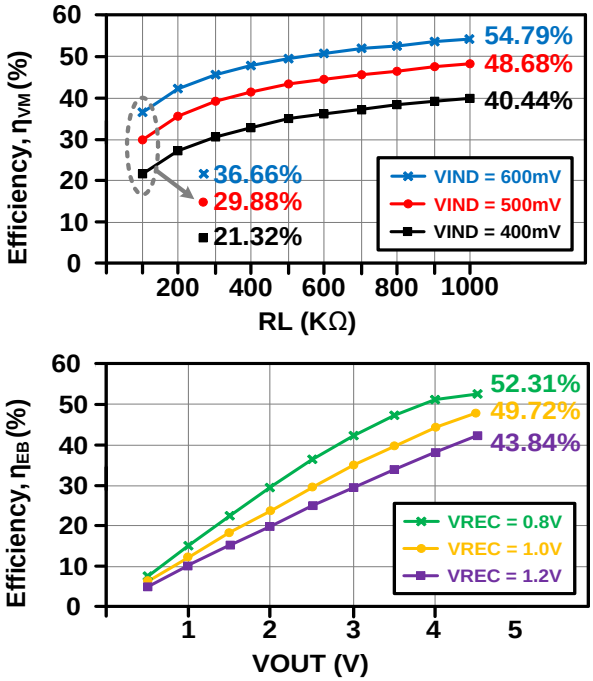


Fig. 8. Power efficiencies of the (a) voltage multiplier and (b) SC energy booster.

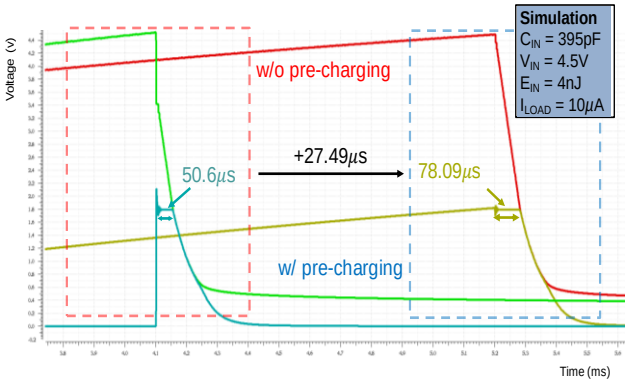


Fig. 9. Waveforms of V_{SC} (a) with and (b) without pre-charging.

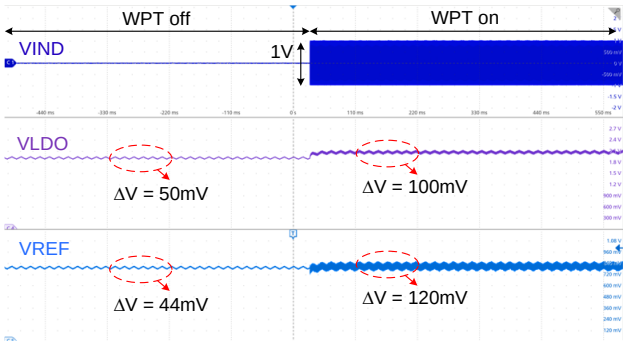


Fig. 10. Inductive noise effects on LDO output voltage.

C. Pre-charging Operation

Fig. 9 shows the simulated V_{SC} waveforms with and without pre-charging. The graph on the left is a result of no pre-charging and shows that the V_{SC} is dropping because the LDO cap is filled. On the other hand, the graph on the right is a result of pre-charging and shows that the LDO operates immediately because the cap of the LDO is pre-charged, and has an operating time of 78.09 μs, which is 27.49 μs higher than the 50.6 μs.

D. Inductive Noise

Fig. 10 is a measurement result on the output voltage of the LDO in the presence or absence of WPT, it can be confirmed that the presence of noise effects by the inductive link. When WPT is off under $C_{L,LDO}$ = 66 nF, V_{LDO} has a ripple of 50 mV. However, when WPT is on, the ripple of V_{LDO} increases to 100mV. V_{REF} shows a similar tendency, increasing from 44 mV to 120 mV depending on WPT on/off. Inductive noise can have a critical impact on the operation of noise-sensitive implantable sensor systems.

E. Chip Micrograph and Comparison

The chip micrograph is shown in Fig. 11. The chip was fabricated in a 180 nm standard process that supports 1.8 V/5 V. The Tx coil has a diameter of 2.5 cm, 4 turns, an inductance of 1.6 μH, and resistance of 3.13 Ω. The Rx coil has a diameter of 0.7 cm, two turns, an inductance of 31 μH, and a resistance of 28.5 mΩ. Table 1 compares the inductive power management system. In this work, a voltage multiplier and step-up SC converter structure are used. It has a 13.56 MHz carrier frequency and can make 4.8 V from 0.5 V AC input voltage. Unlike previous studies, it can store 1152 nJ energy and can sense for 22.25 ms (calculated value) after removing WPT.

V. CONCLUSION

An adaptive power management system is proposed for an implantable sensor system. Since the load power is reduced by turning the circuit on/off according to the phase, it was possible to store high power even with low input power. By using stored power, the internal circuit could be driven even after removing the WPT. Using a passive type supply change circuit, the supply was changed stably and the phase was automatically set according to the voltage with the phase detector. The voltage of the LDO was pre-charged with the pre-charge path so that it could operate for a longer time when the WPT was turned off. The proposed adaptive power management system reduces the noise impact of the inductive link, contributing to more accurate bio-signal measurements.

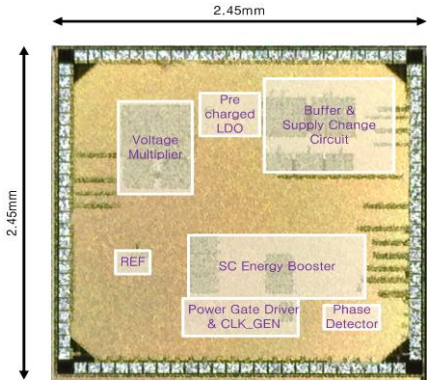


Fig. 11. Chip micrograph.

TABLE I. Performance comparison

Publication	[15]	[16]	[17]	This Work
Technology	0.25-μm	0.18-μm	0.13-μm	0.18-μm
Structure	Voltage multiplier	Voltage multiplier	Voltage multiplier + Step up SC Converter	Voltage multiplier + Step up SC Converter
Carrier frequency	13.56MHz	13.56MHz	433MHz	13.56MHz
V_{AC}	0.5V	0.8V	0.55V	0.5V
V_{OUT}	1.9V	1.8V	2.75V	4.8V
I_{OUT}	10μA	6.67μA	N/A	0.6μA*
Energy Backup	No	No	Yes	Yes (1152nJ)
WPT off at Sensing	No	No	No	Yes (22.25ms**)

* Average current of capacitor charging from 0V - 4.8V
* * At CL,SC = 10nF, ILOAD = 10μA, VSC = 4.8V, VLOAD = 1.8V

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