Design of a GaN-based High Frequency Buck Converter

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***Abstract* - Power management integrated circuit (PMIC) of automotive electrical/electronic components are currently reaching limitations with silicon-based switches. Since the Gallium nitride (GaN) device has a higher power density than the silicon-based TR, it is easy to reduce the size and weight, and is suitable as a power transistor of a switching converter with high frequency operation due to low switching loss and on-resistance loss. Therefore, it is attracting attention as a next-generation power semiconductor device as it can expect effects such as lightening, improving conversion efficiency, and removing dedicated cooling systems when applied to electric vehicles. However, it has structural features different from existing silicon devices, so additional circuit design is required to use it as a switch. This paper relates to a GaN-based buck converter operating at a switching frequency of 10MHz.**
In order to secure the problem of large overvoltage at deadtime due to the absence of a body diode, a block that stabilizes the voltage of the bootstrap (BST) node was added, and the standby current was reduced by using a pulse-driven level shifter. In addition, it operated at a high frequency of 10MHz and used a small inductor of 0.47uH. It was manufactured using the 0.18um high voltage BCDMOS process, and the input voltage is 12V and the output voltage is 5V. The designed area is 2500μm × 2500μm, and the maximum load current is 1A.

***Keywords*—Bootstrap, Buck Converter, GaN, PMIC**

I. INTRODUCTION

In recent years, the power system of automotive electrical/electronic components has reached a limitation due to the use of existing silicon-based power switches. As a result, much attention has been paid to gallium nitride (GaN) power devices to replace silicon-based power switches as the next-generation power semiconductors. GaN switches have a much lower parasitic capacitance component than that silicon device based on on-resistance at the same breakdown voltage [1]. This characteristic means a power converter using a GaN device is run at a much higher switching frequency f_{sw} when compared with that silicon-based power converter with the same efficiency. It also means possible miniaturization of inductors and capacitors at the output terminal.

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Despite these advantages, there are many limits to using GaN devices in the real-world. One of the main limitations is caused by the structural difference from that of silicon devices. A switching node voltage V_{sw} in a general silicon field effect transistor (FET) has a negative value momentarily due to the current flowing in the direction of the output terminal when the low-side power transistor (tr) is at a turn-on state, at which the value does not exceed -0.7V because of the effect of the body diode in the silicon FET. However, because GaN FET has a body diode [2], V_{sw} is dropped to -3V, which may lead to an additional current loss and device destruction. Because of this, an additional circuit, which plays the role of switch in the bootstrap (BST) that turns on the high-side power tr thereby alleviating the voltage drop of V_{sw} node down to -3V.

In Section II. A and B in this paper, the basic operation principle [3] of the buck converter is analyzed and problems, when the power tr of buck converter is used as a GaN device, are discussed. Then, the BST switch, which solves the problems is discussed [4]. In Section II. C, the controller of the designed buck converter is introduced. The voltage mode constant on-time control is applied to this controller, which has a stable transient response characteristic even at a high frequency of 10Mhz [5,6]. In Section II. D, the structure of the gate driver, which directly drives GaN tr of the designed buck converter and the operation principle of each block is described. In addition, the possibility of additional power loss in each block is identified, and the measure to solve the loss is introduced [7-9]. In Section III, the layout of the designed integrated circuit (IC) is explained and the performance and measurement results of the designed GaN-based buck converter are presented. In Section IV, the conclusions and future research of this study are described.

II. DESIGN METHODOLOGY

A. Characteristics of the buck converter using GaN FET

A buck converter is a switching converter, which has a higher efficiency than that of the general linear regulator. It is used as an IC where high power efficiency is important. The main causes of the reduction in power efficiency are a conduction loss of power tr, which is used as a switch, and a switching loss during switching. The conduction loss is a loss consumed when a current flows due to the on-resistance (Ron) of power tr. To reduce the Ron, a large capacity of power tr should be used. The Ron of GaN FET is smaller than that of existing silicon-based devices, which is suitable for a power tr for higher efficiency and has low parasitic

capacitance. Thus, GaN FET is advantageous to run at a higher switching frequency. It has also a high-power density, which is advantageous for lightweight and miniaturization [1]. However, GaN FET has a structural difference from that of silicon-based FET. The difference is that GaN FET has no body diode [2]. To show the role of the body diode in a FET, Fig. 2 shows the graph of voltage change [3,4] in the switch (SW) node of the buck converter.

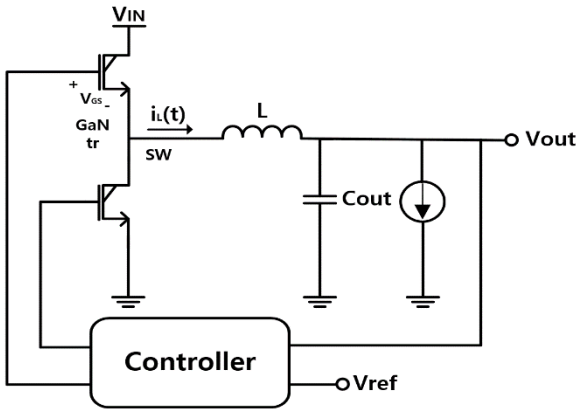


Fig 1. Block diagram of the buck converter using a GaN FET switch

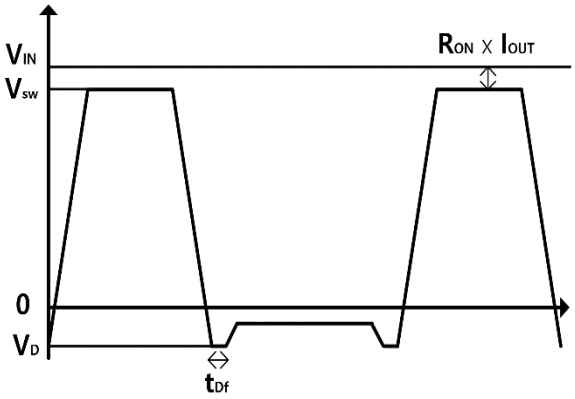


Fig 2. SW node waveform of the buck converter

As shown in the above graph, the SW node changes its voltage as the power tr at the high and low sides is alternately turned on. In particular, because a current flows in the direction from the ground to the SW node direction when the low-side power tr is turned on, - voltage is measured. In addition, there is a t_{df} dead time section where both power transistors are all turned off in the switching section to prevent a shoot-through current, in which a current is consumed as two power transistors are momentarily turned on at the same time during switching. However, because power transistors are all turned off in this dead time section, a current is supplied from the body diode of the low-side power tr. Due to this body diode, V_D voltage is not normally dropped to -0.7V or lower. However, a GaN FET has no body diode so its V_D voltage can be dropped to -2V–-3V. Thus, this problem increases the possibility of destructing the FET by increasing V_{GS} voltage of the high-side power tr. Thus, a block that controls V_{GS} voltage is needed. The principle of the block is explained in the next section.

B. BST voltage and switch of the GaN-based buck converter

A power tr of buck converter normally employs an n-type (-) metal-oxide-semiconductor field-effect transistor (NMOS) that has a small Ron characteristic to obtain higher efficiency. However, when the high-side power tr is an NMOS, a higher gate voltage than the drain voltage should be applied to make the turn-on. Because of this, this study employed the bootstrap technique to generate a 5V higher voltage than that of the SW node. As mentioned above, GaN FET has no body diode, so V_{SW} voltage is dropped to -2V up to -3V in the dead time section [4].

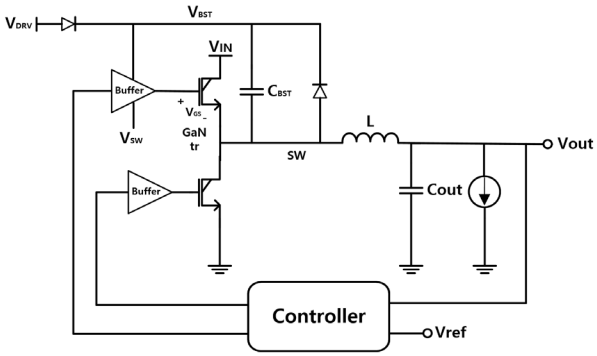


Fig 3. Block diagram of the GaN-based buck converter where BST voltage is applied

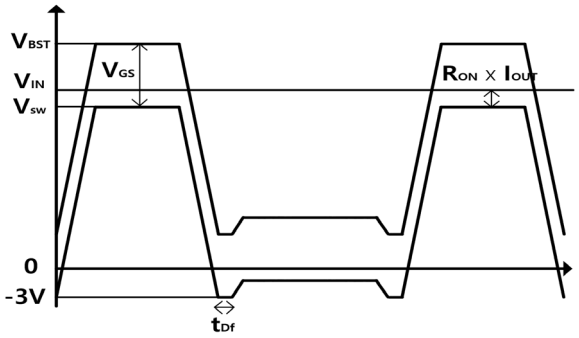


Fig 4. Main switching waveform of the GaN-based buck converter

As shown in the above graph, V_{BST} voltage is one that adds 5V to the SW node voltage waveform of the GaN-based buck converter. However, there is a delay between the BST and SW nodes. Accordingly, when the voltage of the SW node is dropped to -3V, V_{GS} increases to 8V or higher, which is raised above the breakdown voltage of the GaN FET, thereby having a risk of destruction of the FET. Thus, an additional circuit is needed to limit V_{GS} not to exceed the breakdown voltage. In this study, a switch is added to the BST node thereby solving the problem by making the difference between V_{BST} and V_{SW} voltages below 5V.

Using V_{BG} signal and buffer, V_{PGATE} voltage is controlled. Before V_{TG} signal becomes high, V_{PGATE} produces a high signal, thereby interrupting the V_{DRV} voltage supply. Once the voltage supply is interrupted, the voltage charged in C_{BST} is gradually lower from 5V. When the voltage charged in C_{BST} to some extent, V_{SW} voltage is dropped to -3V, and even if there is a delay with V_{TG} signal, V_{GS} voltage does not exceed the breakdown voltage of the GaN FET. The waveforms of the signals are shown in the following graphs.

C. Design of the controller of the GaN-based buck converter

There are two general methods to control a buck converter: current mode control by sensing a current after applying additional blocks to the V_{out} terminal and voltage mode control according to changes in V_{out} voltage. The current mode control configures blocks for sensing an inductor current at the output voltage terminal. The change in the output current in the block is rapidly transferred to the comparator. Because of this, it has the advantage of fast response speed. However, because it employs a resistance using output current sensing blocks, additional power is consumed and it is vulnerable to noise. On the other hand, the voltage mode control has a slower operation speed than V_{out} current mode control and a more complex design of compensator, but it has the advantage of a simpler controller structure [8,9].

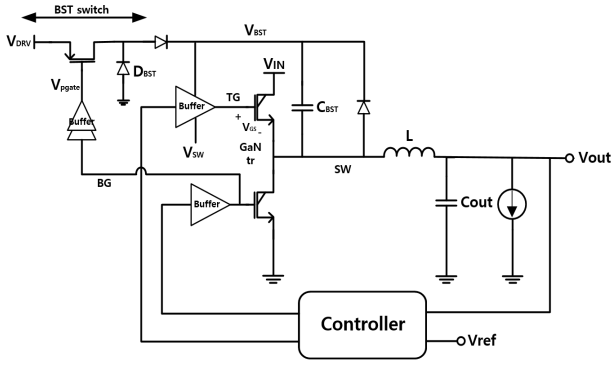


Fig 5. Block diagram of the GaN-based buck converter where BST node switch is applied

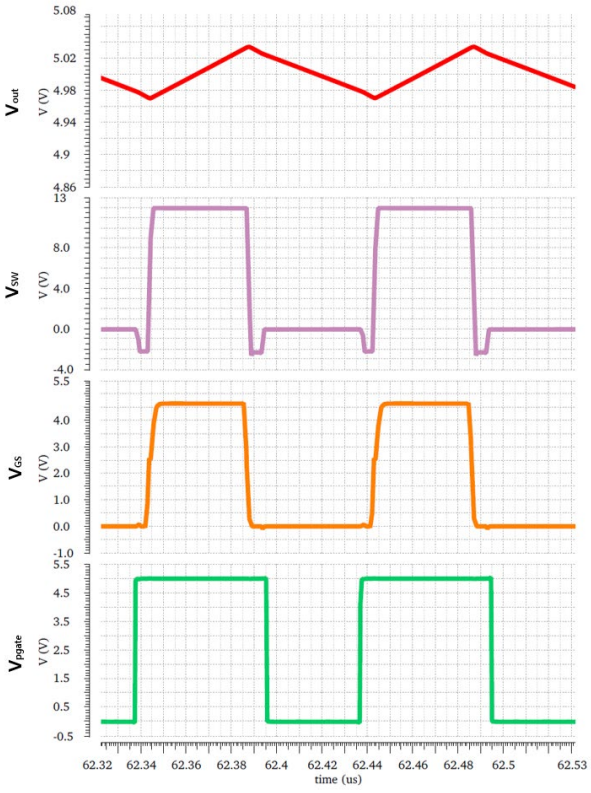


Fig 6. Block waveforms of the BST node switch and main output voltage waveforms

In this study, a constant on-time buck converter where the voltage mode control is applied is designed with a controller. Fig. 7 shows the block diagram of the buck converter where the basic constant on-time control is applied. The controller structure is basically composed of Sr-latch, comparator, and on-timer, and the switching frequency f_{SW} of the controller can be expressed as presented in the following equations [8].

$$f_{sw} = \frac{V_{OUT}}{V_{IN} \cdot T_{ON}} \tag{1}$$

$$f_{sw} = \frac{2L \cdot i_{LOAD} \cdot V_{out}}{T^2_{ON}(V_{IN} - V_{OUT})V_{IN}} \tag{2}$$

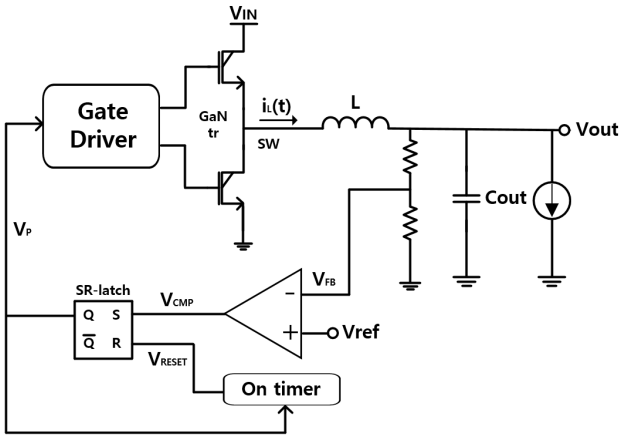


Fig 7. GaN-based buck converter where the constant on-time controller is applied

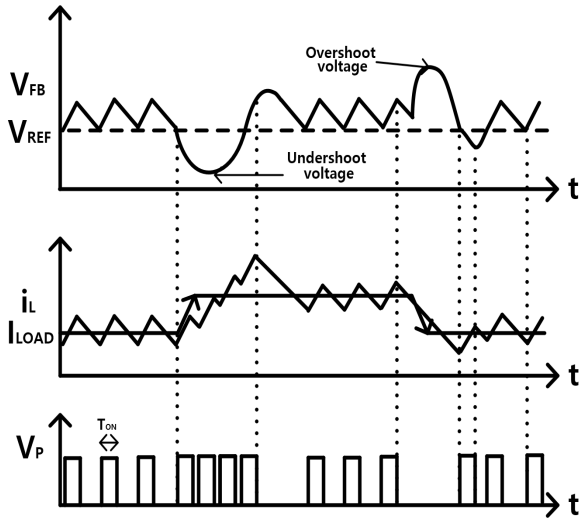


Fig 8. Buck converter waveform using the constant on-time controller

Fig. 8 shows the change in output current I_{LOAD} and waveforms that exhibit the main voltage changes in the constant on-time controller. The principle is that once the output current increases, a current is supplied momentarily from C_{OUT}, and V_{OUT} and V_{FB}voltages decrease. But, due to the negative feedback operation through the controller, the voltage is maintained to V_{FB} voltage. This constant on-time control enables faster charging and discharging of C_{OUT} than that of pulse-width modulation (PWM) control that uses an amplifier, thereby making the operation faster [8]. In the

T_{ON} cycle, the high-side power tr is turned on, which increases the inductor current i_L. Using this, C_{OUT} is charged to increase V_{OUT}. Outside the T_{ON} cycle, the low-side power tr is turned on, thereby decreasing the inductor current i_L, resulting in discharging C_{OUT} and reducing V_{OUT}.

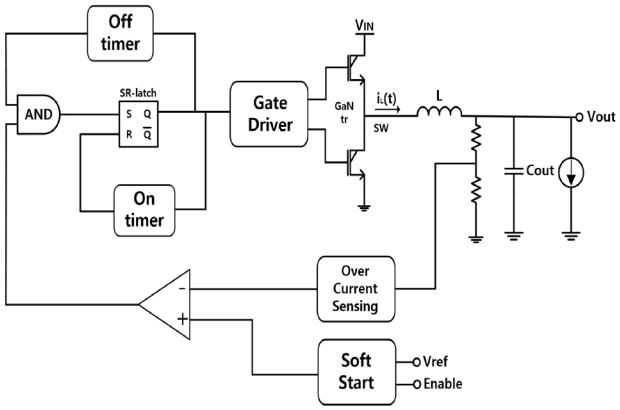


Fig 9. Block diagram of the overall controller of the GaN-based buck converter

As verified in Fig. 9, the overall controller employs an additional soft-start circuit, which prevents the risk of destroying a FET due to the flow of large current such as inrush or overshoot current momentarily by increasing V_{REF} voltage gradually when the initial voltage is applied. In addition, the over-feedback sensor block is also added, which detects a momentary sudden rise of V_{FB} voltage thereby temporarily stopping the operation of the entire circuit.

D. Design of the gate driver of the GaN-based buck converter

The gate driver is a block that directly drives the power tr. The gate driver used in this study was designed to convert inputted PWM signals to signals to drive the switch with a structure that minimizes the additional current consumption and ensures safe driving. The block of the gate driver consists of an up shifter, down shifter, dead time controller, and buffer.

The dead-time controller is a block to prevent a shot-through current by making no turn-on section of large size power transistors at the same time. Using the inputted PWM signals, signals with a dead time of several nanoseconds are produced in the up shifter and low-side buffer.

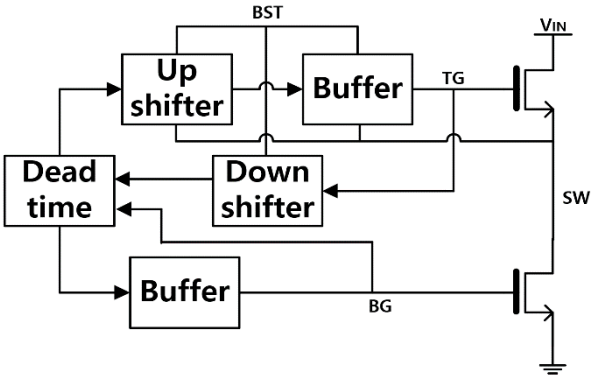


Fig 10. Overall block diagram of the gate driver

The up shifter requires a higher voltage than V_{IN} voltage to drive the high-side power tr. With this required voltage level, it plays a role in up-shifting the signal. This increased voltage level is then inputted to the high-side buffer. The down shifter plays a role in down-shifting the up-shifted signal to a voltage level to be used in the dead time controller. The buffer rapidly charges and discharges a large parasitic capacitance of power tr thereby driving the power tr reliably in the circuit, which is run at a switching frequency of 10MHz.

III. RESULTS AND DISCUSSIONS

The designed GaN-based buck converter is connected to the external GaN device, inductor, and capacitor, and other blocks are all on-chip.Especially, the bootstrap switch, up shifter, down shifter, and buffer were classified as power blocks that switch high voltage from 12V to 17V, and on-timer, off-timer, dead time controller, and soft starter blocks were classified as analog blocks that switch a voltage from 0V to 5V in the layout to reduce interference and noise to each other.

The designed area was 2,500μm × 2,500μm including all power blocks and analog blocks, which were packaged using the chip-on-board method.

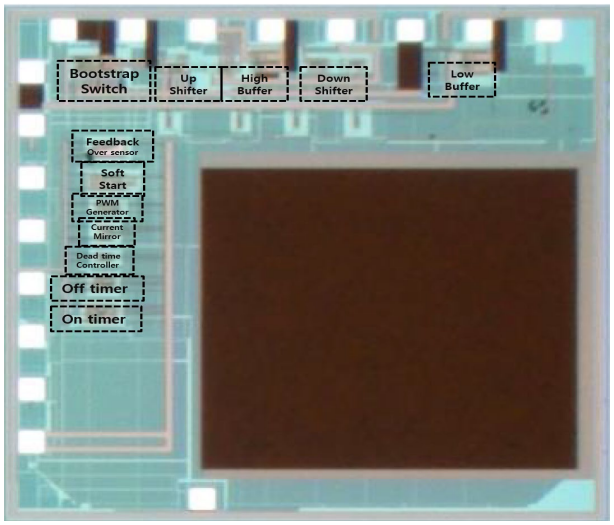


Fig 11. The layout of the designed GaN-based buck converter

Table I. Simulation results and design specifications

Process	TSMC 180nm BCDMOS
Design area	2500um x 2500um
Inductor	0.47uF
Output Capacitor	10uF
Input Voltage	12V
Output Voltage	5V
Switching Frequency	10MHz
Max load current	1A
Efficiency	87%

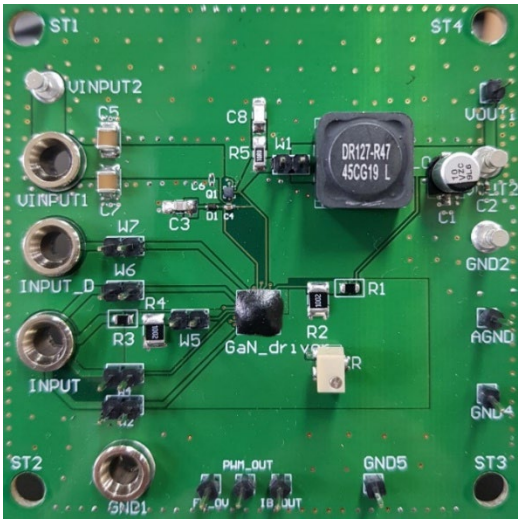
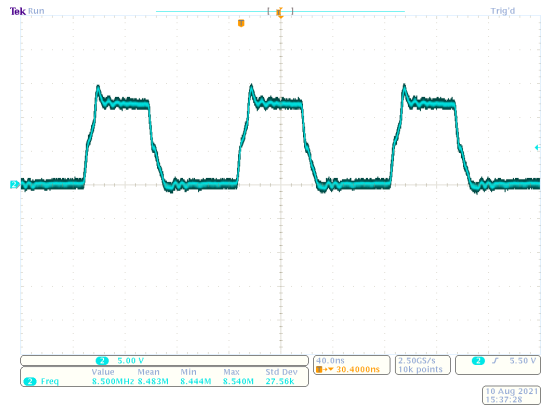
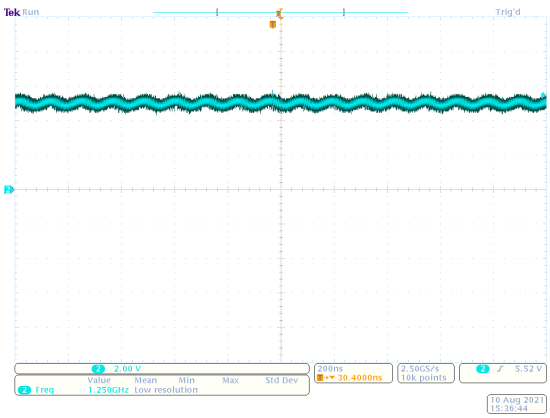


Fig 12. PCB for chip tests

Fig. 12 shows the PCB substrate for chip tests. A test was conducted on the PCB. The surface mount technology was applied to the PCB and COB was also applied. Caps were arranged to reduce the input noise and inductor and caps were arranged in the output terminal too.



(a)



(b)

Fig 13. Chip test V_SW waveform and V_OUT waveform

Fig. 13 shows the V_{SW} and V_{OUT} waveforms observed in the chip test. This figure verifies the normal switching operation where V_{SW} voltage is from 0V to 12V, and V_{OUT} voltage is also produced to 5V.

Table II. Loss Analysis at Maximum Efficiency

Loss	Value
Conduction loss	41.2 mW (1.26 %)
Switching loss	161.2 mW (7.21 %)
Dead time loss	31.2 mW (1 %)
Gate charge loss	1.75 mW (0.12 %)
MOS cap output loss	12.24 mW (0.39 %)
Inductor DCR loss	56.43 mW (1.8 %)
Output Cap ESR loss	5.82 mW (0.25 %)
Efficiency	87%

Table II. analyzes efficiency loss when it has maximum efficiency. The results show that that switching loss is the largest among several losses

IV. CONCLUSION

In this study, a buck converter, which was applied to many power management integrated circuits (PMICs) was designed by applying a GaN switch. The GaN device has a lower Ron component than that of the existing silicon-based device. Thus, it is suitable for a power tr of switching converter that is run at high frequencies, and its power density is low, which is advantageous for lightweight and miniaturization. However, despite that these many advantages, it has a structural difference from existing silicon-based devices. Thus, an additional circuit is needed to use this with existing blocks. The biggest structural difference is that it has no body diode. Thus, V_{SW} voltage can be dropped to around -3V, which makes V_{GS} of power tr large up to 5V momentarily, thereby having a risk of destroying the transistor. As a result, V_{BST} voltage was reduced in the dead time section by using a switch in the BST node in the designed buck converter, thereby removing the risk.

The designed buck converter was manufactured using the $0.18um$ bipolar-CMOS-DMOS process of TSMC, which had $12V$ input and $5V$ output voltages. The maximum load current was $1A$, and because the switching frequency was as high as $10Mhz$, the size of the inductor was reduced as much as that size.

Studies on PMICs using a GaN device, which has been spotlighted as a next-generation power semiconductor device overcoming the limitations of existing silicon devices, will continue to increase as the demand for ultra-small low-power-based tablets and mobile electronics gradually grow in recent years. Thus, the need for the study on applying the GaN device to existing PMICs and commercializing will continue.

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