A Switched-Capacitor DC-DC Converter with Conversion Ratio Controller for Wide Output Power Range

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Abstract **- The DC-DC converter is essential for all modern SoC (System on Chip) to provide proper supply voltage for each system block from the global supply voltage or the energy extracted by the energy harvesting system. Among them, especially IoT (Internet of Things) systems, which are increasing in demand, require DC-DC converters that occupy a small area and cover low-power area. However, the switched-capacitor DC-DC converter has a disadvantage of having a narrow output power range compared to inductor-based DC-DC converters. Therefore, the range of the output load current is limited, which may be a problem in some applications such as light sources driving DC-DC converter. In this paper, we focus on the technique of extending the output power range of the switched-capacitor DC-DC converter. The problems and limitations of the conventional structure were analyzed and based on this, an idea to expand the output power range of the switched-capacitor DC-DC converter was proposed. To prove the effectiveness of the proposed technique, a switched-capacitor DC-DC converter is designed with 65nm CMOS process, and this paper is based on simulations. Various simulations under different conditions were performed, and as a result, wide output load current range of 1 to 20 mA and good power conversion efficiency of up to 80.6% at 1mA output load current are achieved.**

Keywords**—Energy harvesting system (EHS), Inductor-based DC-DC converter, Internet of things (IoT), Switched-capacitor (SC) DC-DC converter**

I. INTRODUCTION

As one system becomes more complex, the voltages required for each block to operate are also diversifying. Therefore, DC-DC converters are added to each block to generate the required voltage with single global supply voltage [1]. Since at least one DC-DC converter is used per block, power conversion efficiency and area of the converter are important. In particular, it is important that the DC-DC converter operates while minimizing power loss as it goes toward low-power applications. DC-DC converters are also used in energy harvesting systems [2,3]. As illustrated in Fig. 1, if a specific device generates power from energy, such as sunlight, RF source, the energy harvester extracts the maximum power and stores the power in the super capacitor or battery. With the stored power, the DC-DC converter generates a stable voltage required for the system.

A switched-capacitor DC-DC converter, charges and discharges the capacitor through periodic switching and creates a specific conversion ratio [4-14]. This type of converter has the advantage of being fully integrated and having less conduction loss. However, there is a limitation in that the range of output power that can be covered is narrower than that of the inductor type.

As mentioned in the previous section, the switched-capacitor DC-DC converter has a limited range of output power that can be covered. This can be a problem in certain applications. For example, a DC-DC converter that drives multiple light sources requires a wide range of output load currents to control many light sources. A new control method of SC DC-DC converter overcoming the limitations with low power consumption is proposed.

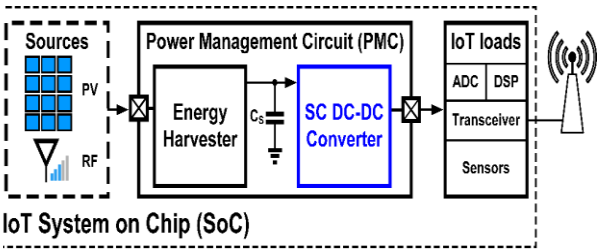

Fig. 1. Switched-capacitor DC-DC converter in IoT system.

II. DESIGN METHODOLOGY

A. Limitation of previous SC DC-DC converter

This section examines the limitations of the existing structure based on the CMOS 65nm process. A converter that receives an input voltage of 0.3 to 1.2 V and generates an output voltage of 0.9 V will be described as an example. Since the conversion ratio is an ideal value without charge loss, a voltage smaller than the value is actually output. Therefore, for example, when the conversion ratio is 1, an input voltage of 0.9 V or more is required to generate an output voltage of 0.9 V. Therefore, the conversion ratio according to the input voltage should be set as shown in Fig. 2.

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Manuscript Received Apr. 21, 2022, Revised May. 25, 2022, Accepted Jun. 5, 2022

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Fig. 3 is to find out what kind of problem occurs when V_{REF1-3} is set in the way described above. The power conversion efficiency according to the input voltage was obtained by changing the conversion ratio and the output load current. Looking at the graph, it can be seen that the appropriate conversion ratio boundary voltage (V_{REF1-3}) differs according to the load current. This can cause two problems when the converter tries to cover a wide range of load currents, which will be explained in detail.

First, it is assumed that V_{REF1} is set based on the 1mA output load current (case 1). Then, as shown on the left side of Fig. 4, it has an optimal power conversion efficiency plot. However, if you take the corresponding V_{REF1} and flow the 10mA output load current, as shown on the right side of Fig. 6, a 'dead zone' occurs that cannot produce the desired voltage no matter how high the switching frequency is raised. To eliminate the dead zone, V_{REF1} must be set high enough to cover the high output load current, which causes another problem (case 2).

Next, it is assumed that V_{REF1} is set based on a high output load current (here, 10 mA) as shown in Fig. 5 (case 2). If V_{REF1} is set high to cover the high output load current, dead zone will disappear. However, the opportunity to achieve higher power conversion efficiency will disappear when the low output load current flows. Thus, the conventional control method is not suitable for covering a wide range of load current because there is a trade-off between the input voltage range and the power conversion efficiency.

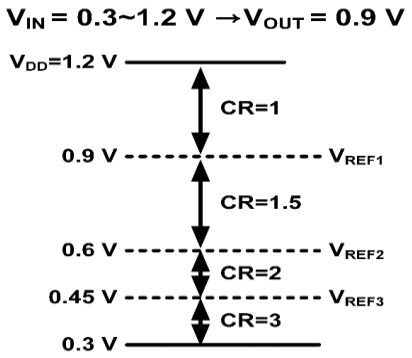


Fig. 2. Input voltage range of previous SC DC-DC converter

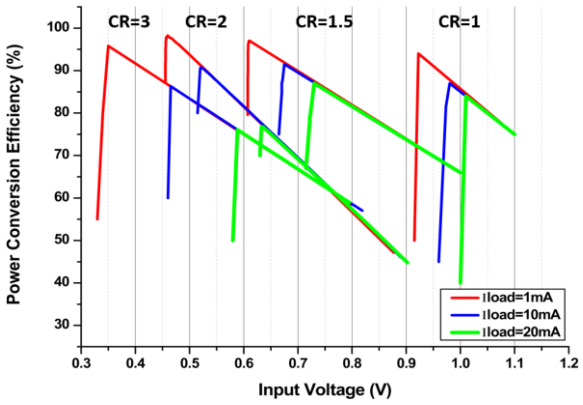


Fig. 3. Power conversion efficiency plot of the SC module with different load current

B. Proposed overall architecture

A new control method is proposed to overcome the limitations of the existing structure mentioned in the previous section. Fig. 6 shows the concept of the proposed structure. Unlike the conventional method, the conversion ratio is determined based on switching frequency information without changing the conversion ratio based on a fixed predefined voltage.

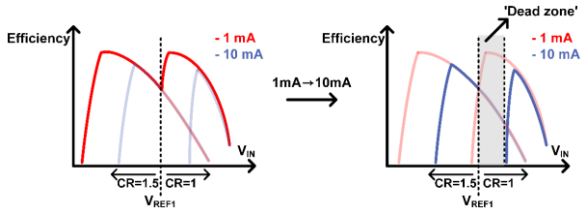


Fig. 4. Limitation of conventional structure-case 1.

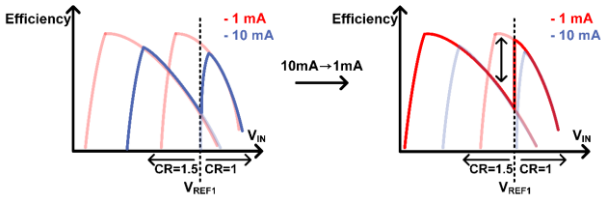


Fig. 5. Limitation of conventional structure-case 2.

First, it operates at the smallest conversion ratio (in this case, 1). If the conversion ratio is insufficient, the switching frequency will continue to increase, and if the switching frequency reaches a preset maximum frequency (f_{max}), the system determines that the current conversion ratio is insufficient and raises the conversion ratio by one step. When the trigger signal appears, it is initialized at the smallest conversion ratio. Like the application mentioned in Section 1.3, the trigger signal may use a signal that exists inside the system, or may input a signal at a specific period depending on the operation speed of applications.

The overall structure of the proposed SC DC-DC converter is shown in Fig. 7. The CR selector part has been changed compared to the conventional structure. Conversion ratio is determined by comparing the output voltage of the charge pump which determines the switching frequency with a predefined upper limit V_{CPmax}. Here, V_{CPmax} is the output voltage of the charge pump when the switching frequency is f_{max}.

The conventional structure requires (N-1) comparators to produce N conversion ratios (in this case, 3 comparators are needed for conventional CR selector). However, with proposed structure, 1 comparator and FSM can handle numerous conversion ratios. It helps to reduce the power consumption of the controller and save chip area.

Fig. 8 shows the flow chart to implement the proposed CR selector. First, the converter operates at the smallest conversion ratio. Then, if the EN signal, which is a signal for initializing the conversion ratio, is not received, the switching frequency is compared to whether the maximum frequency is exceeded. If it does not exceed, maintain the corresponding conversion ratio, and if it exceeds, raise the

conversion ratio one step. After changing the conversion ratio, wait for the COUNT signal from the 9-bit counter to come out to wait for it to be set. By repeating this process, the converter finds an appropriate conversion ratio and continues to operate at the corresponding conversion ratio.

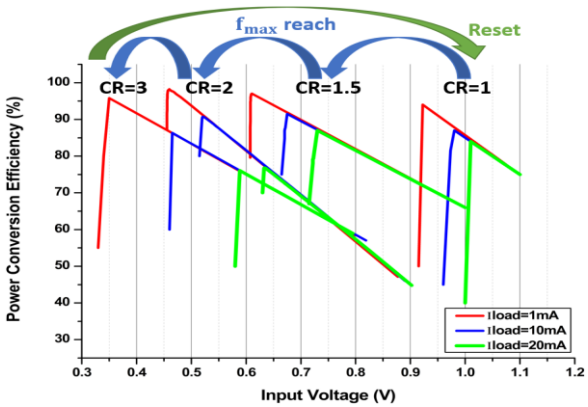


Fig. 6. Concept of the proposed SC DC-DC converter.

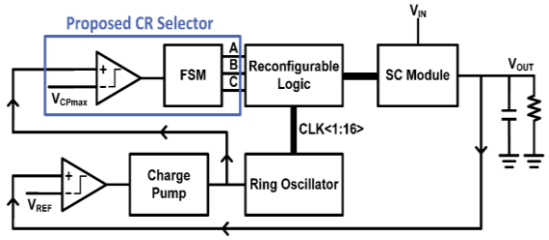


Fig. 7. Proposed block diagram of SC DC-DC converter.

C. Switched-capacitor module

In this design, a reconfigurable SC module structure that supports four conversion ratios (1, 1.5, 2, 3) was used [9]. The schematic of the SC module with the connection state corresponding to each conversion ratio is shown in Fig. 9. Fifteen switches and two MIM capacitors were used. A transmission gates were used on the input side to cover a wide range of input voltages. It was designed by dividing it into 16-unit modules to apply 16 phase-interleaving techniques. Each conversion ratio has optimal frequency range for efficiency in its own input voltage range. The frequency range can be defined by using simulation. Using that information, Voltage-Controlled-Oscillator can be designed properly.

As mentioned in previous section, the capacitor size, which is largely restricted to power conversion efficiency, was used in a given area, and a switch size was determined to have the maximum power conversion efficiency larger than 80% and a decent power conversion efficiency in a wide input voltage range.

D. Comparator

The block diagram of the comparator to be used for CR selector and regulation loop is shown in Fig. 10. It is designed with a dynamic comparator structure, using preamplifier and latch to save static power consumption. First, the preamplifier amplifies the small input difference and the resultant latch makes it low or high to compare the magnitudes of the two input voltages. It is designed to have a resolution of 1 mV or less at a maximum switching frequency by performing overdrive recovery simulation in all input voltage ranges.

E. Charge pump

The schematic of charge pump is shown in Fig. 11. There is a current path that is always on the left branch and flows 20 uA current. The output capacitor is charged or discharged by turning on PMOS or NMOS switch according to CP_{IN}, which is an input voltage of the charge pump, and copying the current flowing through the left branch. A large output capacitor is used to suppress the rapid change of output voltage. If the rising time or falling time of the output voltage is too short, the output voltage would change too fast before the feedback loop is operated, so regulation would not be performed properly.

The differential amplifier in the middle was added in the form of a negative feedback to keep the current flowing through the left branch and the right branch the same. Since the gain of amplifier does not need to be large, this amplifier consists of only one-stage and is designed to use five transistors to obtain a gain of 30 dB or more while flowing a current of 40 uA. The bias voltage of the amplifier is made

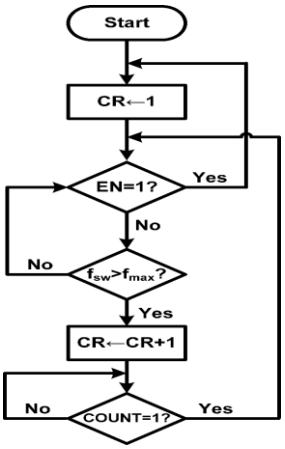


Fig. 8. Flow chart of the proposed SC DC-DC converter

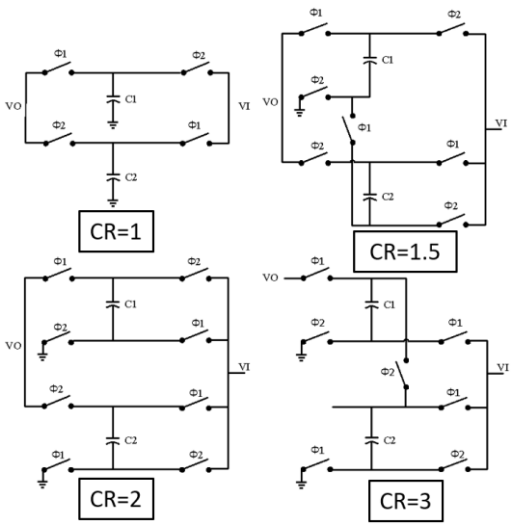


Fig. 9. Reconfigurable of SC module

in the beta multiplier reference (BMR) circuit. Also, compensation capacitor and resistor were added to make the phase margin of this loop above 60 degrees for stability.

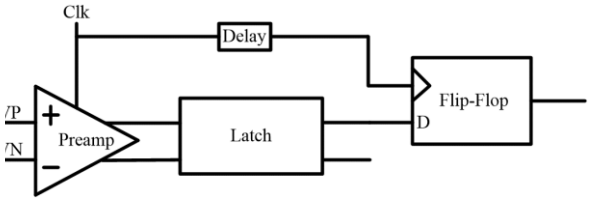


Fig. 10. Block diagram of the dynamic comparator.

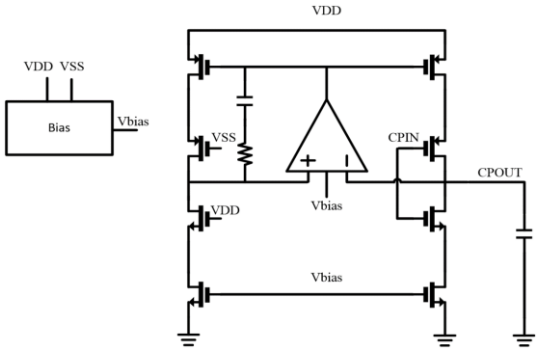
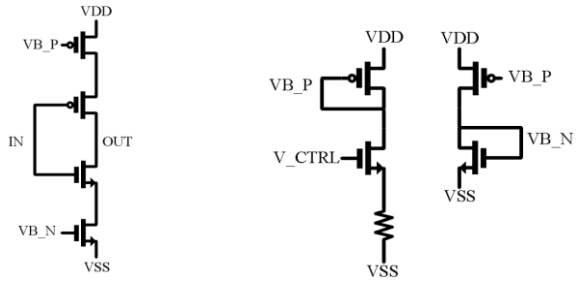


Fig. 11. Block diagram of the charge pump

F. Voltage-controlled oscillator

Fig. 12 shows the schematic of the voltage-controlled oscillator (VCO). The voltage-controlled oscillator is a circuit that generates a clock signal having a frequency proportional to the input voltage. This serves to adjust the output voltage by adjusting the switching frequency in the regulation loop. Since the proposed structure applies a 16-phase interleaving technique, it must generate clock signals with 16 phases. Therefore, a ring oscillator structure in which 33 inverters are configured as a chain is used. At this time, since the frequency is inversely proportional to the delay of the inverter, the current flowing through the inverter is controlled with the input voltage to generate a signal proportional to the frequency.

The schematic of each inverter and control part is shown in Fig. 13. The current flowing by PMOS and NMOS existing above and below the inverter is changed. The current is changed by inserting V_{CTRL} voltage into the gate input of the NMOS of the control part. Resistor is added to the control part to improve linearity between input voltage and the clock frequency.



(a) (b)

Fig. 13. Schematic of (a) the unit inverter and the control part of VCO.

III. RESULTS AND DISCUSSIONS

The proposed structure was designed and verified using a 65-nm 1.2-V CMOS process. The entire chip layout of the proposed structure is shown in Fig. 14. It is measured by simulation. The total area including the pad is 2 mm^2.

The overall timing diagram of the proposed structure is shown in Fig. 15. The first line shows that the output V_O finally follows the V_{REF}. A, B, and C in the middle are the digital codes that determine the conversion ratio. As explained earlier, it initially operates at the smallest conversion ratio and then increases the conversion ratio step by step. Then, if the trigger signal EN signal comes in, it is reset to the lowest conversion ratio. Where illustrated in Fig. 15, since an input voltage of 0.4 V was used, a conversion ratio 3 suitable for generating 0.9 V was finally selected. When the conversion ratio is finally determined, it continues to operate at the corresponding conversion ratio.

Table I shows the controller power breakdown of the proposed structure. It can be seen that the comparators account for a large proportion of the controller power consumption. The proposed structure improves power conversion efficiency by reducing the number of comparators which account for a large portion of the controller power consumption. Also, the additional FSM consumes very little power because it is digital-based block.

Fig. 16 shows the power conversion efficiency of the proposed structure. Up to 80.6% efficiency was achieved when 1 mA load current flows, and up to 75.4% efficiency was achieved when 20 mA flows.

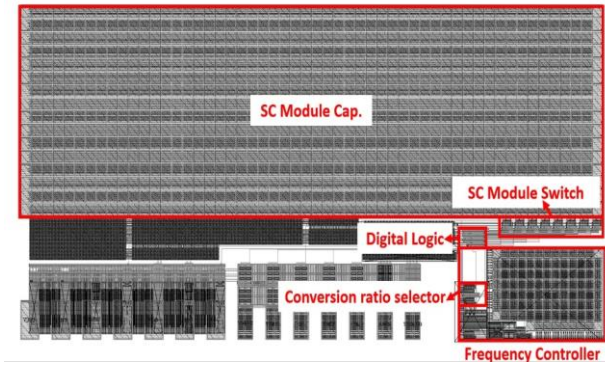


Fig. 14. Top layout of the proposed SC DC-DC converter.

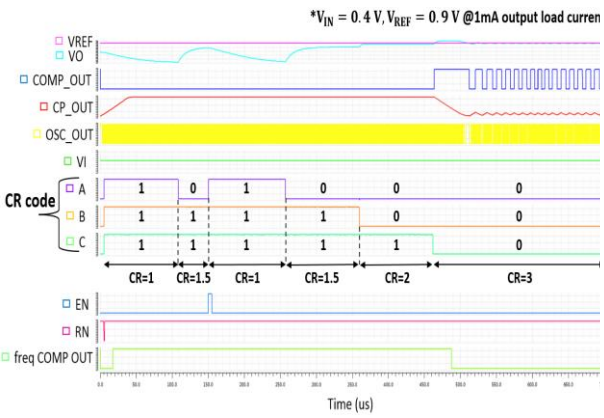


Fig. 15. Timing diagram of the proposed SC DC-DC converter.

TABLE I. Power breakdown of the proposed SC DC-DC converter

	Power Consumption (uW)	Percentage (%)
Charge Pump	84.26	32.1
Frequency Comparator	72.3	27.5
Regulation Comparator	69.91	26.6
VCO	34.43	13.1
FSM+Digital Logic	1.67	0.6

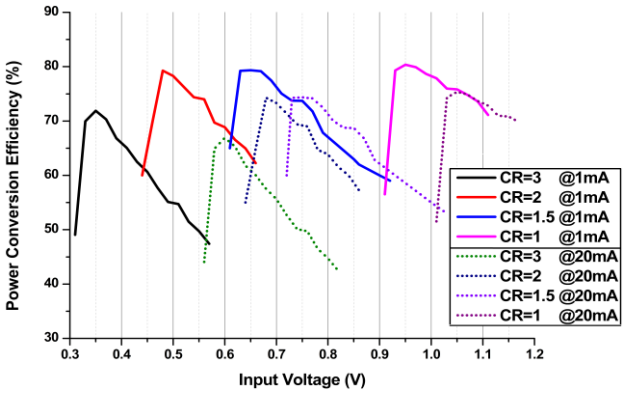


Fig. 16. Power conversion efficiency plot of the proposed SC DC-DC converter.

TABLE II. Performance comparison

	JSCC 2015 [10]	JSSC 2016 [2]	JSCC 2019 [12]	This work
Process	180nm CMOS	180nm CMOS	65nm CMOS	65nm CMOS
Chip Area [mm^2]	0.5	4	1.08	2
Number of CR	2	14	7	4
CR Range	4~6	1.33~8	1.25~5	1~3
Capacitor Type	MOS +MIM	HD +MIM	MOS +MIM	MIM
Load Current [mA]	0.03~ 0.24	0.015	1.2~20.1	1~20
Peak Efficiency [%]	58	81	66.5@1.25mA 80@ 10mA	80.6@1mA 75.4@20mA
Power Density @peak efficiency [Mw/mm^2]	2.4	0.0174	1.16 @1.25mA 9.26 @ 10mA	0.45 @1mA 9 @ 20mA

IV. CONCLUSION

Finally, Table II compares the proposed switched-capacitor DC-DC converter with the structures proposed in the published paper. The proposed structure supports the widest range of load currents among the comparison targets. It also has power conversion efficiency and power density comparable to other tasks. Among them, [12] shows better performance in a wide range of load currents than other structures, and in this reference paper, regulation is controlled externally and focused on the development of SC module.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea

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