Design of an ASK RF Transceiver for ETCs with Hybrid ASK Modulator and Ultra Low Power Wake-Up Receiver

Yeon Jun Kim[1], Jae Hyung Jung, Tae Seob Oh, Jae Bin Kim, Jong Wan Jo, and Kang Yoon Lee[a]
Department of Department of Electrical and Computer Engineering, Sungkyunkwan University
E-mail : [1] cwdw24@skku.edu

***Abstract* - This article presents a CMOS RF transceiver architecture employing Amplitude-Shift-Keying (ASK) modulation for Electrical Toll Collection (ETC) applications. To meet both Korean and Chinese ETC communication standards, the transmitter adopts a hybrid modulation approach. The Korean and Chinese OBU operates at 1024 kbps and 512 kbps, respectively, and the RSU communicates at 256 kbps. By combining digital and analog features, the hybrid structure offers advantages over conventional analog modulators in area, energy efficiency, design portability, voltage scalability, and robustness against process–voltage–temperature (PVT) variation.**

Since Chinese OBUs rely on batteries, minimizing power is a primary concern. The RF transceiver remains in sleep mode until activated by a wake-up receiver (WuRx). To achieve ultra-low-power operation, the WuRx employs an envelope detector with MOSFETs working in the sub-threshold region, allowing continuous operation at extremely low current levels. Digital filtering further improves wake-up detection reliability and prevents false triggers. The WuRx achieves total power consumption of only 3.6 µA.

Unlike conventional receivers with automatic gain control (AGC), ETC receivers must operate reliably without AGC under high-speed vehicle conditions. Therefore, the proposed receiver is designed with a fixed gain yet provides an extended dynamic range of 70 dB. The RX front-end integrates a low-noise amplifier (LNA), a mixer, and a received-signal-strength indicator (RSSI) to achieve robust ASK demodulation while maintaining linearity and compliance with the highest P1dB specification.

The full transceiver is fabricated in 130-nm 1P8M CMOS process with an active area of 3.5 mm × 3.5 mm, including ESD protection.

***Keywords*—ASK, Hybrid approach method, Wide dynamic range**

I. INTRODUCTION

Dedicated short-range communication (DSRC) is short-range wireless communication to provide intelligent transportation system (ITS) services. DSRC is a dedicated short-range communication between a Road-Side Unit (RSU) and an OBU mounted on the vehicle. International companies in South Korea, the United States, Europe, China and Japan are conducting DSRC standardization. DSRC not only provides automatic toll systems, but also provides various services such as traffic information services, road introduction services and logistics services. The main characteristic of DSRC communication is that data transmission is in a narrow field of communication. The implementation of OBU at a small price can not only reduce the investment cost of building the ITS communications infrastructure, but also enable early services to disseminate. Therefore, the terminal hardware/software must be designed with a simple structure and reduced ASIC power consumption. ETC requires user authentication and encryption functions, as well as error-free data transmission to ensure proper charging.

The objective of this article is to design the RF transceiver required for the RSU and the OBU of ETC 5.8 GHz band (Korea-China). It is reported that there are several approaches for the 5.8 GHz DSRC transceiver. Each country requires different specifications. Especially in China, OBU uses batteries not mounted on the vehicle. Therefore, low power consumption is an essential consideration for extending battery life. The first major difference is the speed of the TX data. TX ASK modulators usually use analog modulators [1]-[6]. The analog modulators have limitations in controlling the modulation index and have the disadvantage of causing signal distortion. Reference [6] suggests using an exponential current source for the analog temperature compensation, but consumes more current and layout space. The analog circuit is very vulnerable to PVT variations and the pulse shaping filter requires a large area. Furthermore, larger area is required to support multiple data streams. Compared to the analog one, the ASK digital modulator has lower sensitivity than the PVT and smaller circuit area, but there is the problem of counterfeiting the digital clock [7]. Another difference between the two standards is that WRx only exists in Chinese mode. Since ETC in China is running on battery power, the Always-On module plays a key role in power saving modes such as WuRx, the oscillator and power management circuits. In the case of low power consumption, high WuRx sensitivity, WuRx in the main transmitter and receiver modules, battery life is reduced and overall performance is degraded. Many WuRx circuits have been studied in the literature to optimize energy consumption, maximize sensitivity, and improve reliability [8].

a. Corresponding author; klee@skku.edu

Manuscript Received Feb. 22, 2022, Revised Nov. 20, 2022, Accepted Dev. 19, 2022

This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/by-nc/4.0) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

II. EXPERIMENTS

A. ASK RF Transceiver architecture

Fig. 1 is an upper functional diagram of an RF transceiver for DSRC applications. There is a mode conversion function that supports both Korea and China modes. In China mode, WuRx is still functioning as a module still activated, TRX can only function when it receives the wake-up call. In Korean mode, the WuRX module is disabled and TRX has nothing to do with the wake-up call. The TX module is a hybrid ASK modulator structure based on the power modulator, consisting of a TX, PA and PLL modulator. The RX front block consists of an LNA, a mixer, a polyphase filter (PPF), a filter, an RSSI, an ASK demodulator, there are LDOs that power the circuit, crystal screwdrivers that drives the X-TAL into the circuit, and temperature sensors that compensate the temperature. To support both Korean and Chinese modes, the blocks for changing the setting values are WuRx, TX Modulator, PLL, BPF, and the idea of minimizing the area when changing the mode was proposed. In China mode, the IF signal uses 10 MHz on the low IF structure. In that case, a special case of the image frequency must be received. Therefore, in order to suppress it, the circuit control would be changed. When PLL changes modes in Korea and China, a frequency adapter is used and fast locking technology is adopted. RFC provides fast control signal values when switching between TX and RX modes. SPI communication with the modem. There are temperature sensors, which can adjust the circuit's timing according to the temperature. The temperature condition is confirmed by a numerical value in the modem and the circuit delay is controlled by a value stored in the correspondence table.

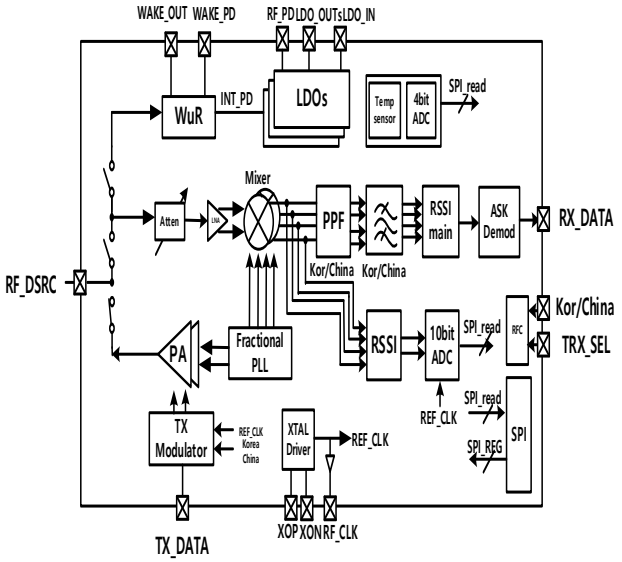


Fig. 1. Top Diagram for DSRC RF Transceiver

B. ASK RF Transceiver architecture

Fig. 2 shows the upper functional diagram of the TX ASK modulator. The TX modulator consists of a pulse shaping controller, an 8-bit DAC, an LPF, a power modulator and a PA.

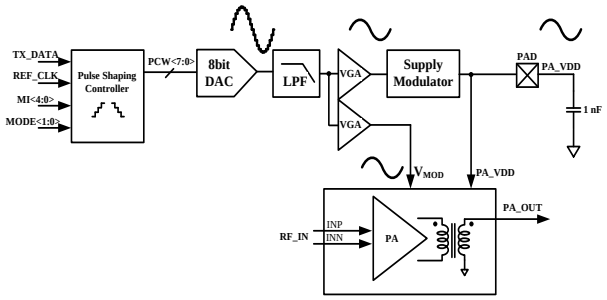


Fig. 2. TX ASK Modulator Top Diagram

C. Wake-up Receiver

Fig. 3 shows the functional pattern of the top of the ultra-low-power wake-up receiver. The wake-up receiver consists of an envelope detector, a gain Stage, comparator, a wake-up receiver controller, ULP BGR, ULP LDO, ULP OSC. The envelope detector detects 5.8 GHz RF signals and generates 14 kHz IF signals. The gain block amplifies the IF signal generated by the envelope detector. The comparator converts the signal generated by the gain stage into a digital signal that the Wakeup receiver controller can recognize. An ultra-low power oscillator operating at 256 kHz.

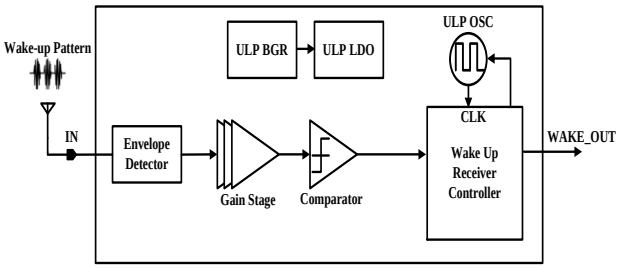


Fig. 3. Top Diagram for Wake-up Receiver

D. Low Noise Amplifier (LNA)

Fig. 4 shows the proposed LNA structure. This study integrates controlled S21 with output capacitors into the LNA. The Cap Bank is controlled by a Class 55F 3-bit hot decoder. The total accordable range is 55F ~ 440F. Thus, the maximum value of LNA band is between 5.5. GHz and 6.1 GHz. The gain control method uses two PMOS connected to the LNA + and - outputs. Using the Ron resistance of PMOS, the charge changes and the gain of the LNA changes. The main structure of the LNA consists of two Common Gate amplifiers with inductive loads. Matching input power (S11) is done internally. For the generated differential signal, the first Common Gate stage provides a 180-degree phase signal, and the second stage reverses the signal again, generating a zero-degree phase shifted signal.

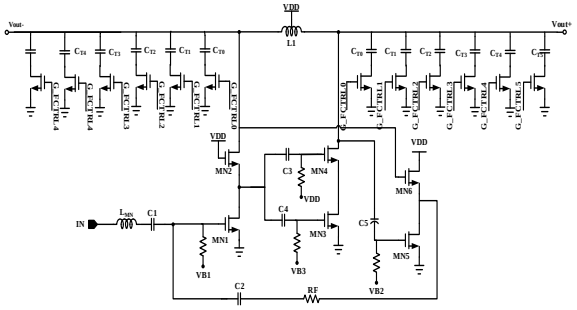


Fig. 4. Top Diagram for LNA

E. Double Balanced Active Mixer

Fig.5 shows the structure of the proposed Double-Balanced Active Mixer. The LO noise voltage is converted into currents of different polarities by pairs of double-balanced switches, summed and suppressed, so that it is less sensitive to LO noise. In addition, using the current mixing technique, the auxiliary transistor is activated at the LO swing intersection, allowing most of the current in the switch pair to flow, thereby reducing the polarization current in the switch pair and reducing the flickering noise. In addition, using PMOS and resistors, the charging stage is realized in the form of a CMFB (Common Mode Feedback circuit), which stabilizes the drain voltage of each switch, prevents the common voltage drop caused by the switch and improves linearity. Furthermore, with limiting the margin, the resistance increases, the conversion gain increases, and the noise value is minimized relative to the existing structure.

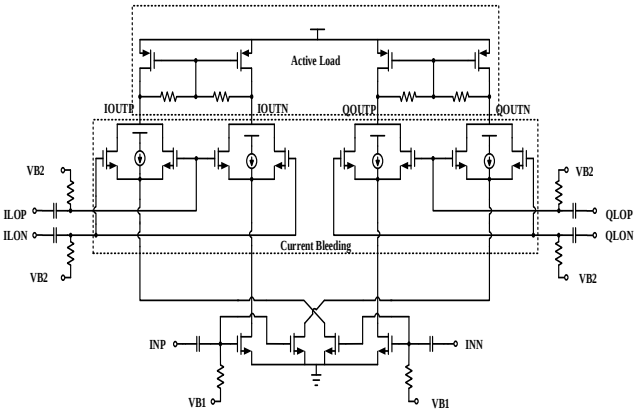


Fig. 5. Proposed Structure for Double Balanced Active Mixer

F. Poly Phase Filter

Fig. 6 shows the proposed polyphase filter structure. Image rejection is only used in Korean mode, so the mode can be changed according to Chinese/Korean mode. The continuous manual RC filter moves the phase, rotates the I and Q signals by 45 degree and separates the desired signal from the image signal, so the image signal can only be attenuated. While the higher the order, the better the image rejection performance, with increasing path loss and amplitude/phase inconsistency, consists of a second step, after image rejection, which maximizes the additional image rejection of the baseband simulation to receive Korean mode signal.

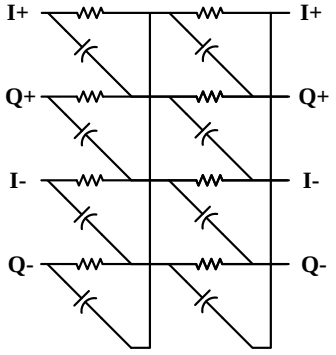


Fig. 6. Schematic Design of Poly Phase Filter

G. Received Signal Strength Indicator (RSSI)

Fig. 7 shows the recommended RSSI block diagram. By implementing a logarithmic function of the RSSI structure, a linear graph of the signal power intensity can be obtained. It is mainly used to monitor input signal power. The circuit is constructed to achieve the final RSSI by connecting the amplitude-limiting amplifier and the on-wave rectifier in series into one unit. Increasing the number of single-cell batteries in series reduces the gain requirement for a single limited current consumption but increases the pole. This results in increased power consumption along with reduced bandwidth. Therefore, considering this issue, the trade-off will take the form of an eight-stage cascade. The cascaded configuration also minimizes the RSSI output error by re-applying the VCM after each step of the input DC offset because DC offset from the front stage is constantly added to the desired signal. Given this straightening step, the bandwidth of the limited amplitude amplifier should allow for a margin.

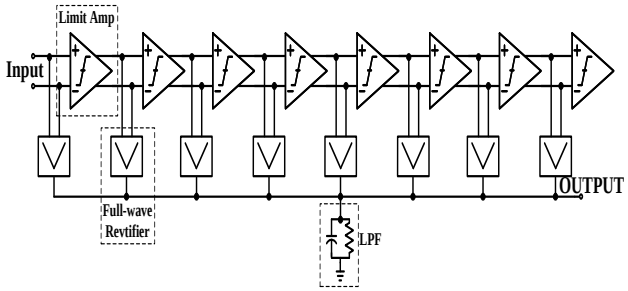


Fig. 7. Proposed Received Signal Strength Indicator Block Diagram

H. Phase Locked Loop (PLL)

Fig. 8 shows a block diagram of the proposed PLL structure. It consists of PFD, CP, VCO, /8TSPC divider, SDM's decimal N divider, and an external third-order loop filter. The proposed simulated phase-locked ring is used as a fraction-N frequency synthesizer with the following frequency output: The counter-N divider parameters (PC, SC, MC) are randomly changed by the delta-Sigma modulator to reduce fractional spurt. It also enables fast locking through Automatic Frequency Correction (AFC) of the digital synthesis module.

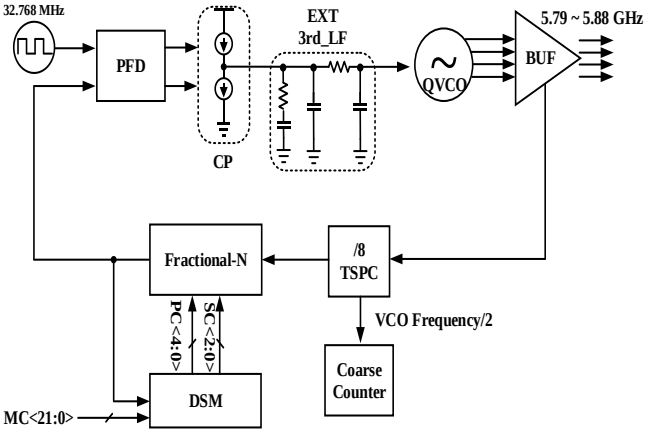


Fig. 8. Block Diagram of analog PLL

To compensate for temperature-related variations in QVCO, a compensating MOS varactor is added. This technology compensates for temperature-related capacitance values in LC tanks by receiving output from PTAT-based temperature sensors. The tail inductance reduces phase noise.

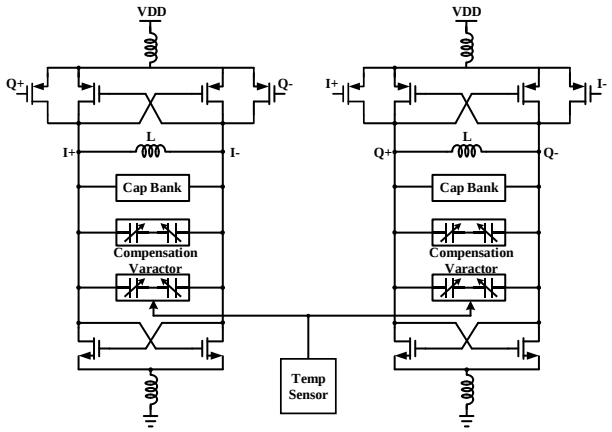


Fig. 9. Schematic of QVCO

III. RESULTS AND DISCUSSIONS

Fig. 10 shows the recommended PCB for the DSRC ASK RF transceiver. It consists of DSRC ASK radio frequency transmission IC, 32.768 MHz crystal, antenna, and TRX common matching network. At 5.8GHz frequency, the distance between the antenna and the chip was shortened to minimize RF port loss, and the number of external devices was reduced, while conventional TRX matching was used.

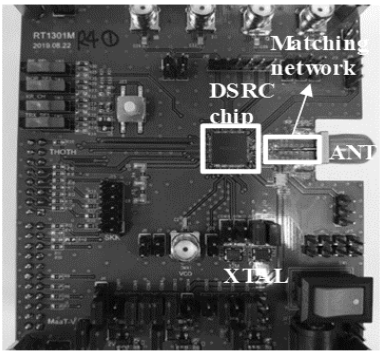


Fig. 10. Measurement board of ASK RF Transceiver

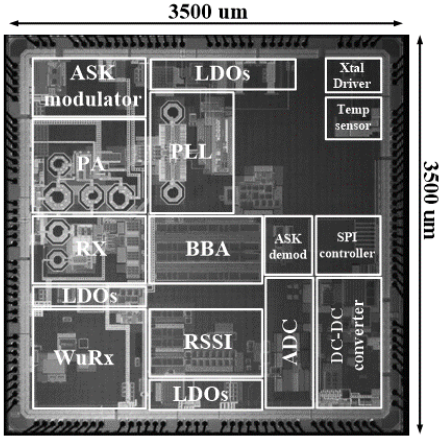


Fig. 11. Layout of the ASK RF transceiver

Fig. 12 shows the measurements in the TX section. RF matching is achieved by S parameters and Smith's circle graphs. If the PA output is set to 6.1 dBm, the reference spurt is 16.384 MHz-43.3 dBc. Finally, the ASK transpose waveform of TX. This is the waveform measured in the time domain where DATA_ is received and TX modulated. Sending IN signals through the modem.

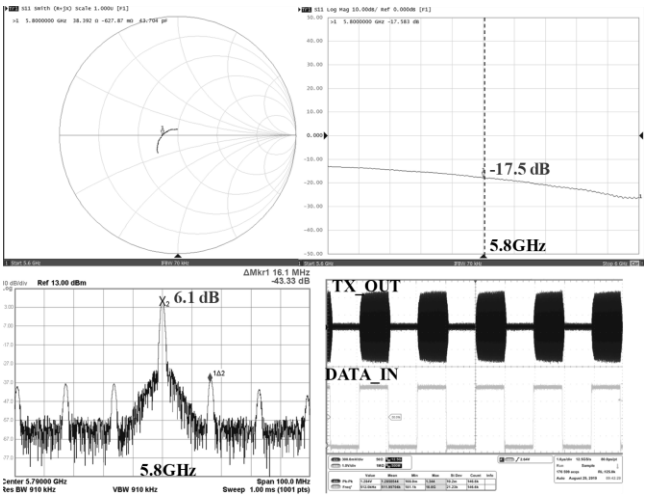
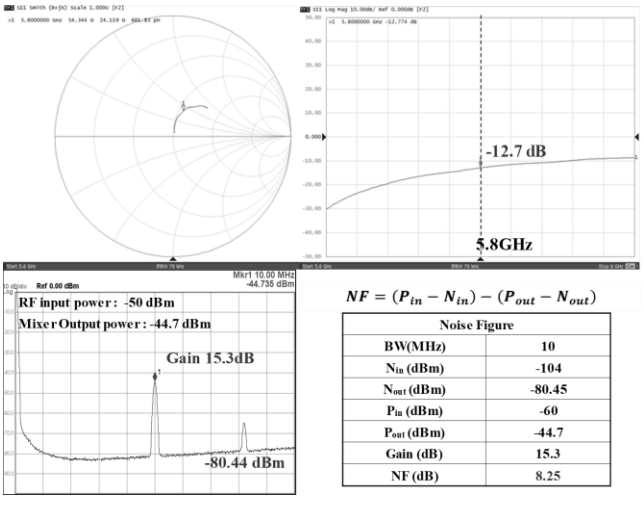


Fig. 12. Measurement result of TX

Fig. 13 shows the measurement results for the RX and BBA components. In RX measurement, use a network parser to measure the S parameters and use the same values to measure the TX status and match the network. The total noise figure for RX is 8.28 dB and the LNA gain is 15.3 dB.

After applying the AM modulated radio frequency signal to the antenna, the oscilloscope confirmed that it outputs a 4-trigger signal through the BBA test port.



$NF = (P_{in} - N_{in}) - (P_{out} - N_{out})$

Noise Figure	
BW(MHz)	10
N_{in} (dBm)	-104
N_{out} (dBm)	-80.45
P_{in} (dBm)	-60
P_{out} (dBm)	-44.7
Gain (dB)	15.3
NF (dB)	8.25

Fig. 13. Measurement result of RX and BBA

Fig. 14 shows the measurements of the Wakeup receiver section. The 14KHz IF signal is fed into the Wakeup receiver through the antenna of the 5.8GHz carrier signal. Wakeup signal is applied periodically. The input number of the OOK signal can be controlled from 1 to 18. Wakeup signal at 5.8GHz and OOK signal at 14kHz are generated at ED_. The OUT signal is processed by digital circuits and the Wakeup signal is generated by the Oscilloscope.

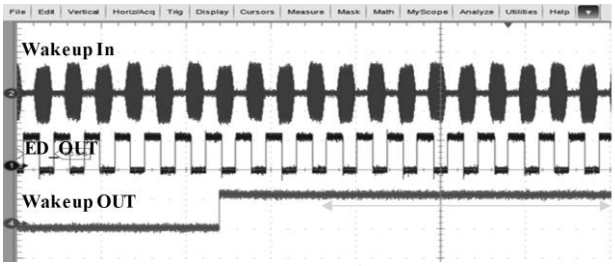


Fig. 14. Measurement result of Wake-up Receiver

TABLE I. Performance Summary

	This Work	[1]	[2]	[3]
Process	0.13um CMOS	0.13um CMOS	0.13um CMOS	0.13um CMOS
Mode	Korea China	China	Korea/Japan	China
RF frequency (GHz)	5.79 ~ 5.84	5.77 ~ 5.84	5.815 ~ 5.845	5.815 ~ 5.845
NF	7.25 dB	-	8 dB	-
TX power	-10 dBm ~ 10dBm	5 dBm	11.7 dBm	-27 dBm ~ 7 dBm
RX data rate	1024 kbps, 256 kbps, 128 kpbs	512 kbps, 256 kbps	1024 kbps	512 kbps
RX sensitivity (dBm)	-88	-85	-80	-86
Current consumption	70mA (TX) 40mA (RX)	46mA(TX) 19mA(RX)	150mA(TX) 52mA(RX)	58 mA(TX)
Modulation index	0.1 ~ 1	0.45~0.95	0.55 ~ 0.96	-
input P1dB(dBm)	-10	-	-41	-
Wakeup sensitivity (dBm)	-60	-44	-	-35
Wakeup Current(uA)	3.6 uA	8 uA	-	15 uA

IV. CONCLUSION

In this paper, an amplitude-shift keying (ASK) radio frequency transceiver structure for the ETC is proposed. To meet Korean and Chinese standards, the TX power modulator proposed a hybrid method. The Korean model is 1024 kbps, the Chinese OBU is 512 kbps, and the Road Side Unit (RSU) is 256 kbps in TX data transfer speed. Hybrid architectures have more advantages in terms of area, power consumption, and PVT variation. China mode ETC is battery powered and power consumption should be reduced. Since the main radio frequency transceiver is switched off until the wake-up receiver (WuRx) receives a wake-up signal from the RSU, the wake-up receiver takes up most of the operation time of the wake-up receiver, minimizing current consumption of the wake-up receiver. In the wake-up receiver, the envelope detector detects the envelope of the wake-up signal using the current characteristic curve of the MOSFET operating in the subthreshold region, so it can operate at ultra-low power consumption. Digital filters are used to improve reliability of wake signals. The total current consumption in the wake-up module is 3.6uA.

ETC communicates when the OBU is high-speed through the RSU. Therefore, RX automatic gain control is not possible. An automatic gain controller is required for normal receivers to avoid saturation of Rx power. However, the ETC cannot adjust the gain and therefore requires a wide range of receiver performance when setting the fixed gain. To satisfy the high P1dB specification and wide Rx dynamic range, the receiver proposes a structure to demodulate ASK signals with LNA, mixer and Receiving Signal Strength Indicators (RSSI). The Rx dynamic range is 70dB. Current consumption for TX and RX is 70mA and 50mA, respectively. The wake-up mode current is consumed 3.6 uA. Wake-up sensitivity is -60dBm. The transceiver is implemented using the 1P8M 130-nm CMOS process and includes an ESD projection pad with a chip area of 3.5mm*3.5mm.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] K. Kwon, J. Choi, J. Choi, Y. Hwang, K. Lee, and J. Ko, “A 5.8 GHz integrated CMOS dedicated short range communication transceiver for the Korea/Japan electronic toll collection system,” *IEEE Trans. Microw. Theory Tech.* vol. 58, no. 11, pp. 2751–2763, 2010.

[2] S. Moazzeni, M. Sawanm, and Glenn E.R. Cowan, “An Ultra-Low-Power Energy-Efficient Dual-Mode Wake-Up Receiver,” *IEEE Trans. Circuits Syst. I Reg.*, vol. 62, no. 2, pp.517–526, Feb. 2015.

[3] T. Polonelli, T.L. Huy, L. Lizzi, F. Ferrero, and M. Magno, “A wake-up receiver with ad-hoc antenna co-design for wearable applications,” in *IEEE Sensors Applications Symposium*, Catania, Italy, pp. 20–22, Apr. 2016.

[4] J. Blanckenstein, J. Klaue, and H. Karl, “A Survey of Low-Power Transceivers and Their Applications,” *IEEE Circuits Syst.* Mag., vol. 15, no. 3, pp. 6-17, thirdquarter 2015.

[5] Research Institute of Highway Ministry. *Electronic Toll Collection-Dedicated Short-Range Communication-Part 1: Physical Layer*; China Nat. Standard GB/T 20851.1-2007, Research Institute of Highway Ministry: Beijing, China, 2007.

[6] H. Liu, X. Qu, L. Cao, R. Liu, Y. Zhang, M. Zhang, X. Li, W. Wang, and C. Lu, “A 5.8 GHz DSRC digitally controlled CMOS RF-SoC transceiver for China ETC” *in IEEE Asia and South Pacific Design Automation Conference*, Jeju, Korea, pp. 22–25, Jan. 2018.

[7] Noboru Sasho *et al.*, “Single-chip 5.8GHz DSRC transceiver with dual-mode of ASK and Pi/4-QPSK,” in *IEEE Radio and Wireless Symposium*, Orlando, FL, USA, pp. 22–24, Jan. 2008.

[8] J. Choi, I-Y. Lee, K. Lee, S-O. Yun, J. Kim, J. Ko, G. Yoon, S-G. Lee, “A 5.8-GHz DSRC transceiver with a 10-μA interference-aware wake-up receiver for the Chinese ETCS,” *IEEE Trans. Microw. Theory Tech.* vol. 62, no. 12, pp. 3146–3160, Dec. 2014.

Yeon Jun Kim received his B.S. degree from the Department of Electrical Engineering at Sungkyunkwan University, Suwon, Korea, in 2022. He is currently working toward the M.S. course in Electronics and Computer Engineering from Sungkyunkwan University, Suwon, Korea. His research interests include LNA and Switch.

Jae Hyung Jung received his B.S. degree from the Department of Electrical Engineering at Kookmin University, Seoul, Korea, in 2022. He is currently working toward the M.S. course in Electronics and Computer Engineering from Sungkyunkwan University, Suwon, Korea. His research interests include PLL.

Tae Seob Oh received his B.S. degree from the Department of Mathematics at Sungkyunkwan University, Suwon, Korea, in 2020. He is currently working toward the M.S. course in Electronics and Computer Engineering from Sungkyunkwan University, Suwon, Korea. His research interests include DAC and Analog filter.

Jae Bin Kim received his B.S. degree from the Department of Electrical Engineering at Myongji University, Suwon, Korea, in 2019. Since then he has been working toward the combined Ph.D. & M.S. Course in electronics and computer engineering from Sungkyunkwan University, Suwon, Korea. His research interests include RF Energy Harvesting and Wireless Power Transfer System.

Jong Wan Jo received his B.S. degree from the Department of Electronic Engineering at Cheongju University, Cheongju, Korea, in 2018. He is currently working toward the M.S degree in School of Information and Communication Engineering, Sungkyunkwan University. His research interests include Wireless Power Transfer systems and Power Management IC.

Kang Yoon Lee received the B.S., M.S. and Ph.D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively

From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, where he was a Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University as an Associate Professor. Since 2012, he has been with College of Information and Communication Engineering, Sungkyunkwan University, where he is currently a Professor. His research interests include implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.