# An On-Chip Cockcroft-Walton Switched-Capacitor Converter Using Split-Phase Control for Improved Soft-Charging with 9.72 Conversion Gain

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*Abstract* - **This work proposes a switched-capacitor (SC) converter for high voltage generation required for medical ultrasound imaging system. The SC converter is quite advantageous for the implementation of an integrated circuit (IC) in terms of area. Besides, the SC converter has relatively less conduction loss than an inductive DC-DC boost converter. For these reasons, the SC converter is suitable for generating high voltages in ICs. However, the power loss of the SC converter can be analyzed by dividing it into three major losses. This work analyzes these losses and applies techniques to reduce them in order to improve the conversion gain and power efficiency. As a result, an on-chip Cockcroft-Walton SC converter using split-phase control for improved soft-charging with conversion gain 9.72 and power efficiency 70.1% suitable for the portable ultrasound imaging device is implemented. However, the measurement results of this study were worse than the simulation results due to mismatched control clock.**

*Keywords*—**Cockcroft-Walton (CW) topology, Split-phase control, Soft-charging, Switched-Capacitor (SC) converter**

## I. INTRODUCTION

Step-up DC-DC power converter is electronic circuit that converts lower dc voltage levels to higher dc voltage levels by storing the input energy to energy storage components and transferring the stored energy to the output. These circuits are essential to several kind of applications that require higher voltage than supply voltage. Step-up DC-DC power converters can be largely classified into inductor-based DC-DC boost converter using inductor as energy storage and switched-capacitor (SC) converters using capacitors as energy storage [1]. SC converters have some advantages and disadvantages compared to inductor-based DC-DC boost converters.

Capacitor has a greater energy density in the same area than inductor. Besides, capacitor can be integrated more easily than inductors. Unlike the inductor-based DC-DC boost converter that employs magnetic energy storage, SC converter employs only switches and capacitors. Inductor-based DC-DC boost converter requires a bulky power inductor and high voltage (HV) devices that requires a large area. Therefore, SC converter is quite advantageous for the implementation of an integrated circuit (IC) in terms of area.

Also, SC converter has relatively less conduction losses than inductive DC-DC boost converter [3]. In case of the DC-DC boost converter, voltage stress of switch is the difference between input DC voltage ($V_{IN}$) and output DC voltage ($V_{OUT}$). If the conversion gain ($V_{OUT}/V_{IN}$) is high, the switches of DC-DC converter should be used as an HV devices. However, the voltage stress applied to each switch of SC converter is the same as $2V_{IN}$, so there is no need to use HV devices even if the conversion gain increases. Therefore, the DC-DC boost converter that has to use HV devices has a relatively high on resistance. And even considering the number of SC converter switches, conduction losses of DC-DC boost converter tend to be large under high conversion gain conditions. For this reason, SC converter is more advantageous in implementing high voltage generation into ICs than inductor-based DC-DC boost converters. And it is widely used in biomedical applications where chip size is quite important factor [4]-[7].

SC converter has low switch-related losses due to the low resistance of the switches aforementioned. However, the SC converter generates a high voltage by accumulating charge on the capacitors. When flying capacitors are connected to each other during operation, large current spikes occur momentarily due to voltage mismatch of flying capacitors, as seen in Fig. 1. These current spikes are charge redistribution losses and it is the main reason of deteriorating power efficiency of SC converters.

Power loss of the SC converter can be analyzed by dividing it into three major losses. As shown in the Fig. 2, charge redistribution losses are dominant at low frequencies, switching losses are dominant at high frequencies and conduction losses are proportional to total resistance of switches. Charge redistribution losses are inversely proportional to the capacitance $Cfly$. And, the change of charge in the flying capacitor is proportional to the duration of the charge & discharge. Thus, these losses are inversely proportional to the switching frequency $fsw$ [8]. Switching loss is the switched-related loss and this is proportional to the switching frequency ($fsw$), gate capacitance of switches

($Cgg$), the number of switches ($Nsw$), a width of a switch i ($Wi$), a length of switch i ($Li$), and the square of the gate-source voltage of switch i ($Vgs,i$). Lastly, conduction losses are proportional to total resistance of switches ($Ron$).
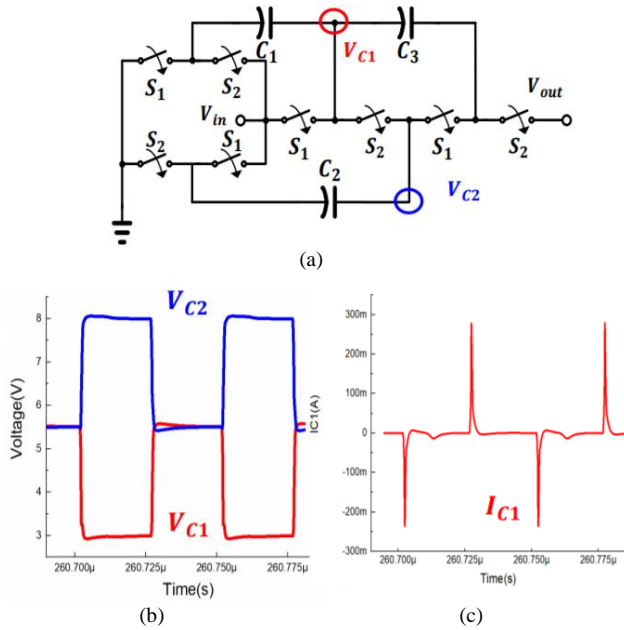


(a)



(b)                    (c)

Fig. 1. Simulation results of charge redistribution losses (a) Circuit of SC converter (b) Node voltage of flying capacitor 1, 2 (c) Current waveform in charge redistribution process

Recently, there are various SC converters with soft-charging technique, which can eliminate the transient current spikes by adding an inductor [2], [8]-[9]. When the inductor is inserted in the current path, rapid current change does not occur by the inductor. As a result, lossless regulation is enabled and the transient current spikes is eliminated in SC converters. As charge redistribution losses are reduced, the critical point moves to a lower frequency region. Through soft-charging operation, switching losses can be reduced by lowering the switching frequency, and the overall power loss can be improved by reducing transient current spikes caused by charge redistribution. Adding inductor also prevents transient inrush currents which incur significant losses in conventional SC converters.
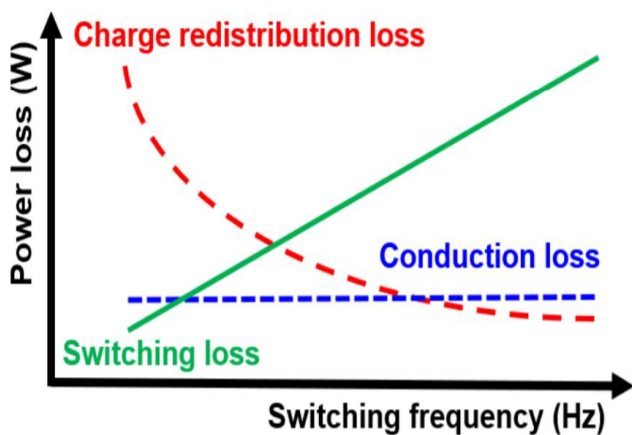


Fig. 2. Power losses of a typical SC converter

Considering all three main loss, a critical point ($f_{crit}$) is switching frequency with minimal losses. In conventional SC converter, the critical point is inversely proportional to capacitance of flying capacitors, resistance of switches $R_{on}$, and device parameter $k$

$$f_{crit} = \frac{1}{2\pi k(R_{on}C_{fly})} \quad (1.1)$$

In soft-charging SC converter, critical point (1.1) is modified due to the inductor, and a modified critical point is given by (1.2), as seen in Fig. 3.

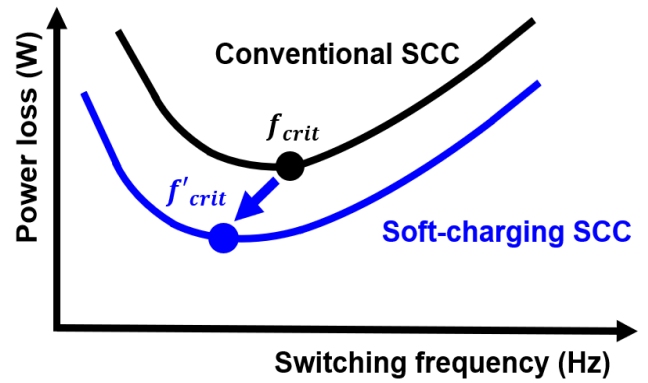$$f'_{crit} = \frac{1}{2\pi\sqrt{LC_{fly}}} \quad (1.2)$$



Fig. 3. Overall power loss of SC converter with soft-charging operation

The DC-DC boost converter uses the inductor to store energy, so it needs high Q power inductor to reduce DC loss and it can't use small inductors because of their low Q. But the SC converters use the inductor to smooth out the current peak, so do not need such high Q inductor. Thus, SC converters can use very small inductors. Therefore, by using soft-charging operation, the power efficiency of SC converter is improved by reducing the two types of power loss. The goal of this study is to design an on-chip SC converter that has greatly improved the power efficiency by applying soft-charging technique.

II. DESIGN METHODOLOGY

A. *Cockcroft-Walton (C-W) topology*

There are several topologies of SC converter with high conversion gain. When the conversion gain is N, the voltage stress of the flying capacitors and switches of each topology is as follows. The voltage stress of capacitors and switches of Cockcroft-Walton (C-W) topology is $2V_{in}$, $2V_{in}$, respectively. C-W topology, where the low voltage stress is applied to all devices regardless of the number of stages, are most suitable for on-chip high-voltage applications than other topologies. In the case of this topology, soft-charging technique is performed by inserting the inductor into the input node. The reason for inserting the inductor into the input node is as follows. The only node that the inductor can serve as a current source without breaking the current path is the input node. Although there is no previous research that applied split-phase soft-charging control to Cockcroft-

Walton topology, it is expected that power loss reduction would be significant due to a similar structure of Dickson topology [8]. Therefore, this study applies soft-charging using the split-phase control to the Cockcroft-Walton SC converter to create a high voltage and improved the power efficiency significantly.

### B. Soft-charging technique with split-phase control

Before explaining the split-phase control, let's take a look at the basic operation of the Cockcroft-Walton SC converter. In the case of a basic SC converter with conversion gain 6, the odd-numbered switches and the even-numbered switches alternately turn on/off and accumulate charge in the flying capacitor, as seen in Fig. 4 and Fig. 5. The input voltage is 3 V, clock frequency is 10MHz, the size of switches is same and all flying capacitors are same.
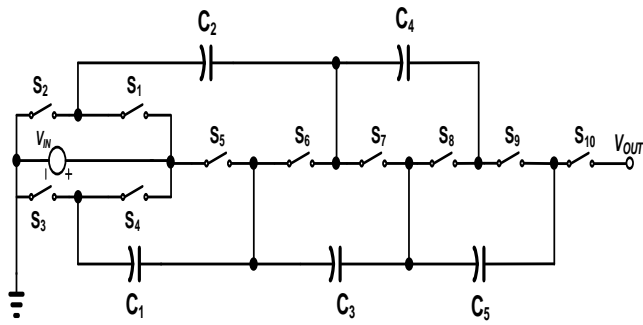


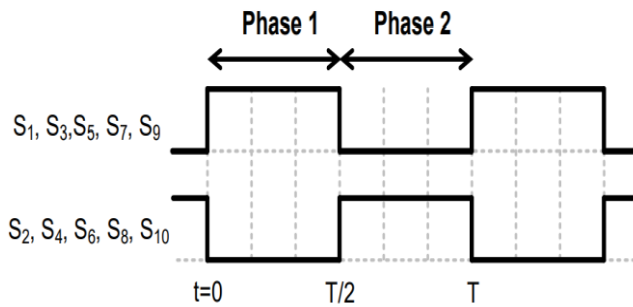Fig. 4. Circuit of a basic C-W SC converter with conversion gain 6



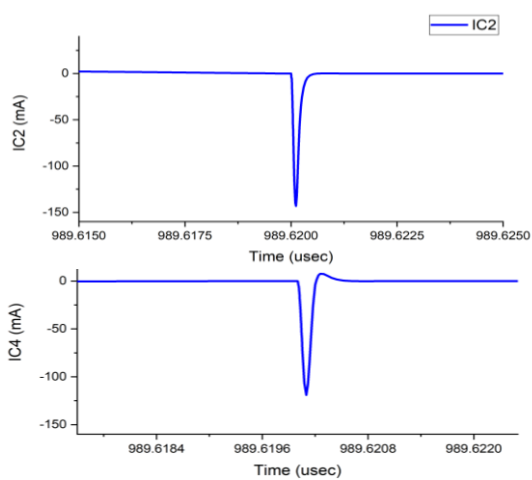Fig. 5. Two-phase clock used in C-W SC converter



Fig. 6. Transient current spike in conventional C-W SC converter using two-phase control

The inductor current of phase 1 flows only through $C_1$, so the KVL (Kirchhoff's Voltage Law) condition is slowly adjusted by the inductor current even if there is a voltage mismatches among capacitors and the transient current spike of capacitor $C_1$ is not severe. However, in the case of capacitors except $C_1$, when transitioning from phase 2 to phase 1, charge redistribution occurs instantaneously between capacitors, resulting in a transient current spike over 120mA, as seen in Fig. 6. Therefore, phases that smoothly match the voltage mismatches between capacitors using the inductor current are needed.
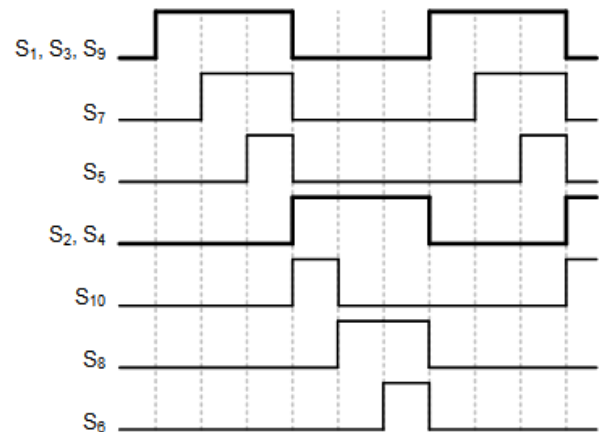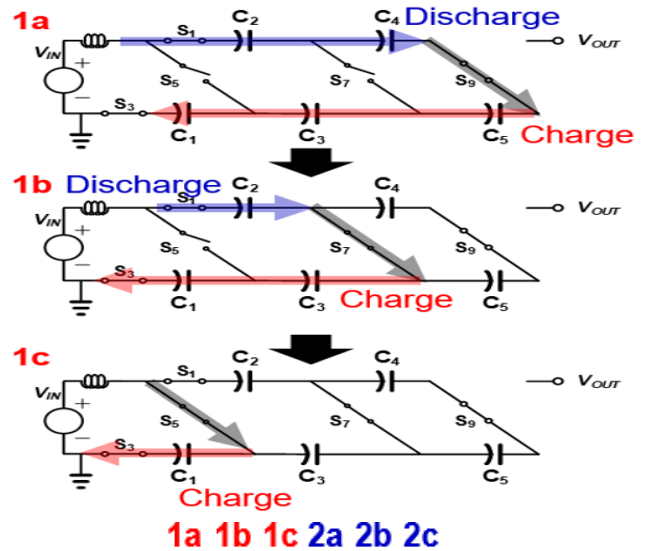


Fig. 7. Example of split-phase control for C-W SC converter

The additional phases are needed that makes the voltage of $C_2$ and $C_3$ the same, and the phase that makes the voltage of $C_4$ and $C_5$ the same. The phases added and node voltages when transitioning from phase 2 to phase 1. Phase 1a makes the voltage of $C_4$ and $C_5$ the same, phase 1b makes the voltage of $C_2$ and $C_3$. When the voltages of $C_2$ and $C_3$ are same, phase 1c closes S6 and finishes the phase 1. The node voltage can be smoothly changed by closing the switches sequentially from the outside. Through this, the transient current spikes are reduced from above 120mA to below 30mA, as seen in Fig. 8.

## C. Proposed soft-charging C-W SC converter

Target specification is selected by referring to ultrasound transducer driving that requires high voltage, as seen in Fig. 9. The input voltage is set to 3 V, and the target output voltage is 30 V. The allowable error of the output voltage is set to 10%, which is a minimum of 27 V and a maximum of 33 V. When using the RC modeling of the piezo-electrical transducer referenced, the ultrasound pulser instantaneously uses 1.5 A for 50 ns, and the period of corresponding pulse is 50 $\mu$s. Based on these, the DC average current obtained by calculating the average output power is 1.25 mA, so this is selected as the load current target. The switching frequency is selected between $10 - 60$ MHz, which is the operating frequency band of a general ultrasound imaging system. When using 1.5 A in the load with an output voltage of 30 V, the output capacitance that can keep the ripple within 3 V is about 30 nF, so output capacitance is set to 30 nF. And the critical point is set to about 20 MHz by setting the inductor to 1 $\mu$H

The control circuit excluding the SC converter core is largely as follows: a split-phase clock generation block, a clock-retimer that synchronizes the generated split-phase clock, and a level shifter that raises the voltage level so that split-phase clock can turn on/off the core switch, as seen in Fig. 10.

The split-phase clock generation block makes control signals, as seen in Fig. 7. If each clock overlaps when the phase is changed, short circuit current flow through the switches and the efficiency is greatly reduced. Since the probability of the clocks overlapping due to PVT (Process,
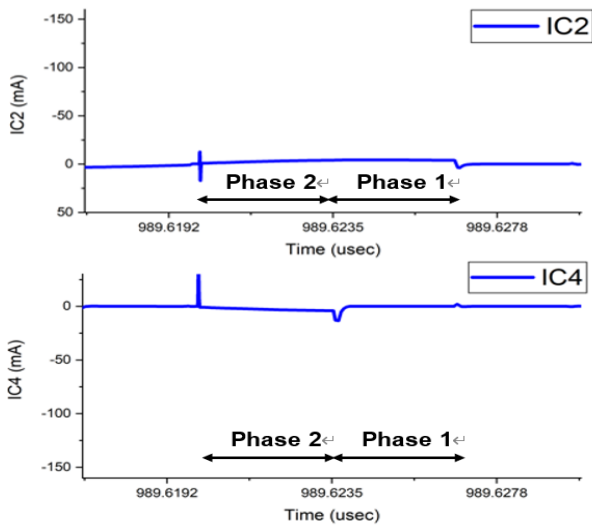


Fig. 8. Transient current spikes in soft-charging C-W SC converter using split-phase control
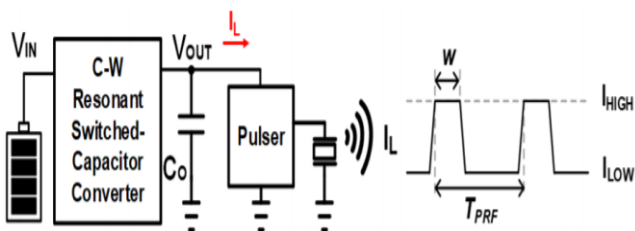


Fig. 9. Specifications to drive the pulser for ultrasound transducer.

Voltage, Temperature) variation is high, such a clock timer is essential. It needs to raise the voltage level to use it in the soft-charging Cockcroft-Walton SC converter core. to 3 V. Since the voltage stored in the flying capacitor of the SC converter core is 6 V, which is twice the input voltage 3 V, a 6 V clock is required, and the generated clock is used in a high voltage level shifter.
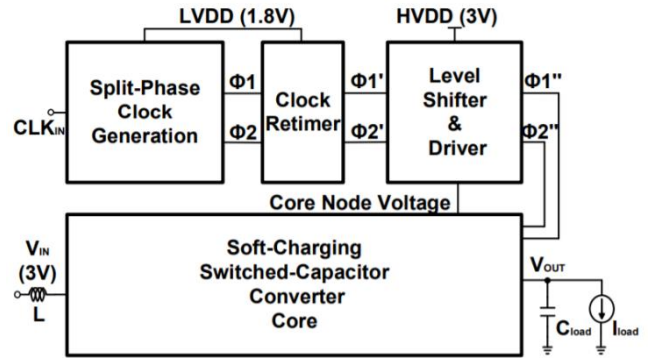


Fig. 10. Block diagram of soft-charging Cockcroft-Walton SC converter

## III. RESULTS AND DISCUSSIONS

The comparison target is divided into three cases: hard-charging with the two-phase control, soft charging with the two-phase control, and soft-charging with the proposed split-phase control. In each case, the switching frequency and load current are changed and the power efficiency and conversion gain are calculated and plotted as a graph. The transient current spikes mentioned in chapter II is compared for 3 cases. In the two-phase control soft-charging that added only the inductor to the input node, the transient current spikes improved slightly, as seen in Fig. 11.

As shown in Fig. 12, in terms of power efficiency, there is no significant improvement compared to two-phase hard-charging when using two-phase soft charging control. However, the power efficiency and conversion gain improve by applying the proposed split-phase control scheme. Peak efficiency of hard charging with two-phase control is 43.48% at 0.5- mA load current, 10 MHz switching frequency. And peak efficiency of soft charging with two-phase control is 51.11% at 1.5-mA load current, 10 MHz switching frequency. Lastly, peak efficiency of soft charging with proposed split-phase control is 75.17% at 0.5-mA load current, 10 MHz switching frequency. It can be seen that both soft-charging SC converter with split-phase and two-
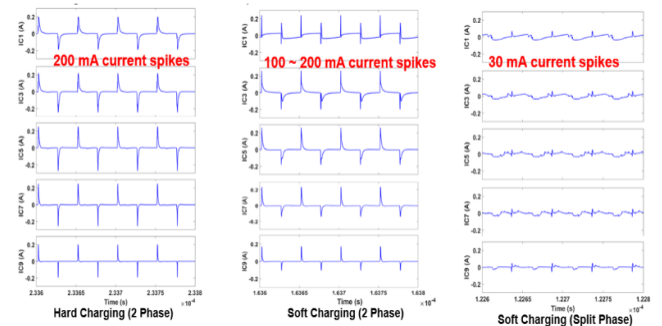


Fig. 11. Charge redistribution loss in SC converter with 3 different control technique

phase control reduce charge redistribution losses and achieved a higher conversion gain than the hard-charging control. Soft-charging SC converter with split-phase has the highest power efficiency at all frequency.
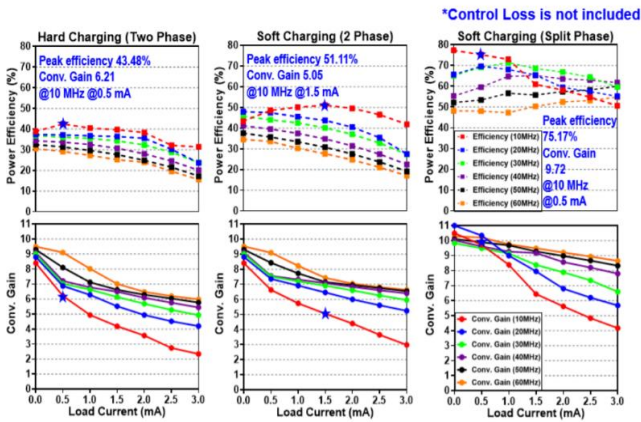


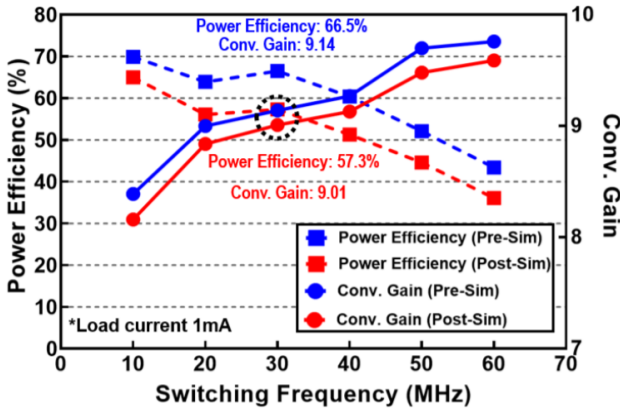Fig. 12. Simulation results of power efficiency and conversion gain without control loss
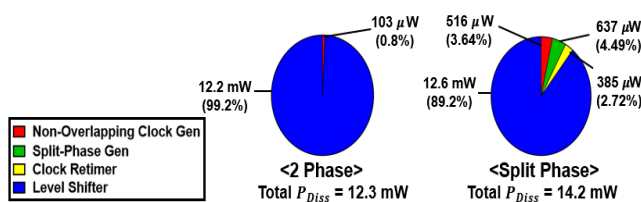


Fig 13. Post-layout simulation result



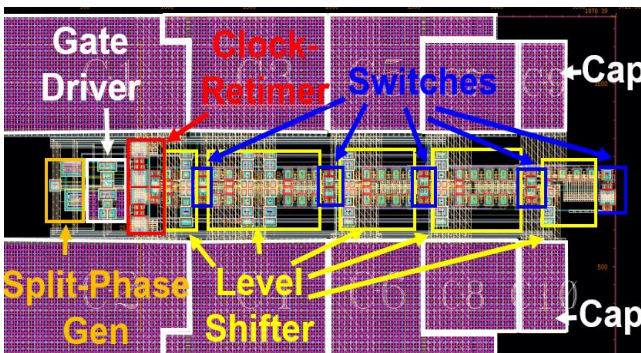Fig 14. Power consumption of the C-W SC converter control circuit



Fig 15. Layout of soft-charging Cockcroft-Walton SC converter (without pads)

Fig. 13 is the post-layout simulation result. Compared with the previous simulation, the power efficiency and conversion gain of the post-layout simulation is inferior. This is because the interconnection metal wire is too thick. So, power losses due to parasitic capacitance are severe. From this result, the switching frequency should be changed from 20 MHz to 30 MHz at 1-mA load current. Compared with the previous simulation, the power efficiency decreased from 66.5% to 57.3%, and the conversion gain decreased from 9.14 to 9.01. As shown in Fig. 14, the two-phase control does not require blocks related to the split-phase clock, so most of the power consumption is generated by the level shifter. Split-phase control consumes about 90% of the power by the level shifter. The layout of the soft-charging Cockcroft-Walton SC converter core with pads is 4.37 mm x 2.35mm, as shown in Fig. 15.

TABLE I. Comparison with other SC converters

|  | TCAS II 2019 [11] | APEC 2015 [12] | ISSCC 2014 [13] | This Work |
|---|---|---|---|---|
| $V_{IN}$ | 2.8 V | 33 V | 2.75 V | 3 V |
| $V_{OUT}$ | 12.8 V (x4.57) @1-mA load current | 117 V (x3.54) @1.5-A load current | 30 V (x10.9) @10-μA load current | 29.16 V (x9.72)* @0.5-mA load current |
| Peak Efficiency | 84.7% @2-mA load current | 92% @1.1-A load current | 38% @25-μA load current | 70.1 %* @0.5-mA load current |
| $f_{SW}$ | 100 kHz | 1.2 MHz | 8 MHz | 20 MHz |
| $I_{LOAD}$ Range | 0.5 mA ~ 2.0 mA | ~ 2.25 A | ~ 25 μA | 0.5 mA ~ 2.5 mA |
| Topology | Latched | Dickson | Doubler + Dickson | Cockcroft-Walton |
| Clocking Scheme | 2 phase | Split phase | 4 phase, 2 phase | Split phase |
| Total Flying Capacitor | 8 x 1 μF (SMD) | 4 x 0.1 μF (SMD-1812) | 400 pF (on-chip) | 6 nF (on-chip) |
| Inductor | X | 100 nH (5.5mm x 5.18mm) | X | 1 μH (SMD-0603) |
| Technology | 0.18 μm | 8 x GaN FET (Discrete) | 65 nm | 0.18 μm BCD |

In the case of the first TCAS II 2019 paper [11], the load current range is similar but conversion gain is 4.57. It is hard-charging with two-phase control and the total flying capacitance used as a large value of 8 μF by using the SMD (Surface Mount Device) type. As a result, the switching frequency is lowered to 100 kHz, resulting in a high efficiency 85%. However, this is because the conversion gain is low, so the number of stages is low and charge redistribution loss and switch-related loss is low.

In the APEC 2015 paper [12], the split-phase control is applied to the SC converter with low conversion gain. Although the topology is different from TCAS II 2019 paper, 92% power efficiency is achieved by applying split-phase control despite using the low flying capacitance. Because GaN FET with low resistance and SMD type capacitors with high capacitance, power efficiency is very high. The disadvantage of this paper is that total area is quite large due to discrete devices. Comparing these two papers [11]-[12], differences between the off-chip SC converter with hard-charging control and the off-chip SC converter with soft-charging control can be seen.

Let′s look at the case of the SC converter implemented on-chip. ISSCC 2014 paper [13] is a fully integrated SC converter. Doubler and Dickson topology is used in succession, and conversion gain and switching frequency are similar to this work. However, the peak efficiency is as low as 38%, and load current range is too low.

However, this work achieves conversion gain of 10 and

can drive a load current up to 2.5 mA. And a relatively high efficiency of 70% is achieved as the integrated SC converter. Disadvantage of this work is that the inductor used in the SC converter is discrete device.

## IV. CONCLUSION

In this work, we proposed a method to improve the soft-charging of the Cockcroft-Walton SC converter through split-phase control. The power efficiency and conversion gain are further improved through optimization of the switching sequence of the split-phase clock. Through this method, a conversion gain of 9.7 and a power efficiency of 70% are achieved. As a result of post layout simulation at 1-mA load current, 53.1% power efficiency and a conversion gain of 9 are achieved, which is reduced compared to pre-simulation.

The measurement results of this study were worse than the simulation results due to mismatched control clock. It should be designed in consideration of how to prevent this problem. This chip was designed using TSMC 0.18μm BCD process.

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