A CMOS LiDAR Sensor OEIC for Elder-Care Systems

Ji Eun Joo[1], Myung Jae Lee and Sung Min Park[a]
[1]Department of Electronic and Electrical Engineering, Ewha Womans University
[2]Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology
E-mail : [1]wxop01@naver.com

***Abstract* – In this paper, an optoelectronic integrated circuit (OEIC) by utilizing a 180-nm CMOS technology for a linear LiDAR sensor in the applications of elder-care systems is presented. It consists of an on-chip avalanche photodiode (APD) a voltage-mode linear transimpedance amplifier, a post-amplifier, a limiting amplifier, and a 50-Ω buffer. Post-layout simulation results show that the proposed OEIC achieves 96-dBΩ transimpedance gain, 780-MHz bandwidth even with 3-pF photodiode capacitance, 5.08-pA/√Hz noise current spectral density, and 29.2-mW power dissipation. The entire chip includes 4-channel arrays, hence occupying the area of 2.0 x 2.5 mm^2 together with I/O pads.**

***Keywords*—Avalanche photodiode, CMOS, Elder-care, LiDAR, Optoelectronic IC**

I. INTRODUCTION

Recently, the population of single-elders and senile dementia patients has been globally increased owing to the results of aging societies. It has consequently led to tremendous social costs for elder care service, particularly in the developed countries such as R. O. Korea because of the life longevity benefitted from its advanced health care system and distinguished economic growth.

In 2012, the Ministry of Health-Welfare in South Korea predicted that one-million elders (10 % of senior citizens) might suffer dementia in 2025. In accordance with this prediction, the extremely high cost of two trillion won might have to be spent to treat these infirm elders. Currently, the portion of single elders in their fifties and sixties has become more than 20 percent in the population of South Korea.

Either these single elders or senile dementia patients have tendency of being easily troubled with declining cognitive ability. They tend to face the dangers of falling accidents, heart attack during sleep, even suicide [1]. In particular, the falling accidents of elders occur mostly in their houses and that more than 40-% of falling accidents happen to those older than 80 years. Worse is that two-third of the elderly patients over 85 years old end up with facing death. Fig. 1 reveals the death from falling accidents among those aged over 65 years old in the US from 2007 to 2016.

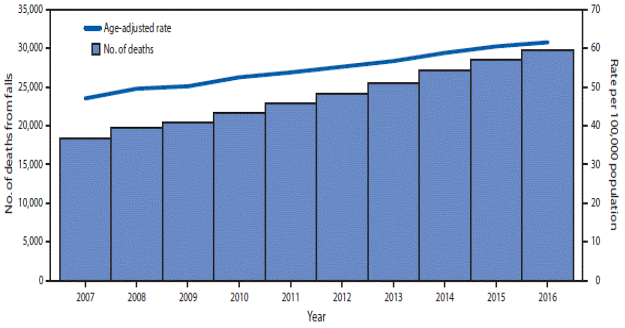

Fig. 1. Statistics of death from falling accidents in US from 2007 to 2016.

Besides, single elders are frequently afraid of heart attack during sleep and many other serious illnesses on their own. Some of them may be lucky to live with their family, but it is still difficult to avoid the unexpected situations of sudden death from heart attack and suicide. For the purpose to take care of these senior citizens who live alone or those who suffer dementia, the Korean government and many social well-fare centers have organized systematic monitoring systems such as visiting nurses, senior care centers, emergency notification services, etc. However, we strongly believe that it is better to equip electronic sensors in their houses and send alarms instantly to either their family or visiting nurses in real-time for the sake of their precious life.

A survey conducted for senior citizens indicates that they loathe a huge-size monitoring system, e.g., CCTV, because it can observe their ordinary lives with sharp images and thus violate portrait right. Hence, electronic monitoring sensors for elders are required to be very small, invisibly equipped at a corner of a ceiling, and provide depth information in emergency, thus alarming the situations promptly to families and nurses.

For these purposes, a small, low-power, low-cost LiDAR (light detection and ranging) sensor can be a better solution not only because it can yield blurred images, thus avoiding portrait right violation, but also because it can precisely provide mandatory information of elders that includes falling accidents [2,3]. In this paper, we present a CMOS analog front-end (AFE) circuit with on-chip avalanche photodiode (APD) integrated to realize a required LiDAR sensor for elder-care systems.

When a LiDAR sensor is integrated with optical detectors, it provides a number of advantages over conventional RF sensors due to its robustness against large RF interference [4,5]. Also, CMOS on-chip optical detectors are very

a. Corresponding author; smpark@ewha.ac.kr

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attractive because they can lower the total cost of multi-channel modules under the condition that the on-chip APD should yield appropriate optical responsivity. Certainly, it should be noted that the wavelength of 850 nm is utilized for these CMOS silicon APDs and that it can be detrimental to eye-safety with large power emission.

II. OEIC ARCHITECTURE

Fig. 2 depicts the overview of the proposed LiDAR sensor for elders. It consists of a multi-channel CMOS analog optoelectronic integrated circuit (OEIC) array with on-chip APD. First, the transmitter (Tx) emits a light pulse to a target (a single elder in this figure). The reflected light pulse enters the OEIC, which converts the light pulse into a digital code in the end, so that either the distance to the target or its depth information can be easily estimated. The 3-D images of a targeted single elder can be achieved by utilizing FPGA-based verification process. Then, the images will be delivered to family/nurses in real-time, thus avoiding feasible dangerous outcome from falling and suicide.

Fig. 3 shows the overall architecture of a single-channel OEIC receiver (oRx) which comprises an on-chip silicon APD, a voltage-mode CMOS feedforward transimpedance amplifier (VCF-TIA), a single-to-differential (S2D) conversion circuit with a passive low-pass filter (LPF), two-stage additional gain-cells, a cascaded limiting amplifier (LA) with a DC voltage offset cancellation network, and an output buffer (OB) for 50-Ω impedance matching. The on-chip APD is realized in a spatially-modulated configuration, as described in [6] because it blocks the part of active area using a metal layer to subtract slow diffusion currents of the photodetector. Therefore, the bandwidth is typically extended, however, at the expense of its responsivity [7].

III. RESULTS AND DISCUSSIONS

A. Circuit Description

Fig. 4 depicts the schematic diagram of the VCF-TIA that includes a feedforward network, i.e., a common-source amplifier with a gate resistor (R_g) to avoid unnecessary oscillation occurred from a parasitic bond-wire inductance and a comparatively large input photodiode capacitance. In this configuration, the drain voltage of M_3 is identical to those of M_1 and M_2 due to the resistive feedback inverter.

Therefore, the larger the resistance of R_L is, the more the DC current of M_2 flows. This results in a boosted g_{m2}, hence leading to the decrease of the noise contribution from M_2. Also, it can alleviate the design tradeoff between gain and bandwidth owing to the decreased input resistance. Therefore, the feedback resistance (R_f) can be set higher than that of a conventional inverter TIA, while maintaining the same bandwidth [2].

A S2D converter is followed to pass the single-ended output voltage over to a fully-differential LA. The cascaded 2-stage LA employs both negative-resistance and negative-

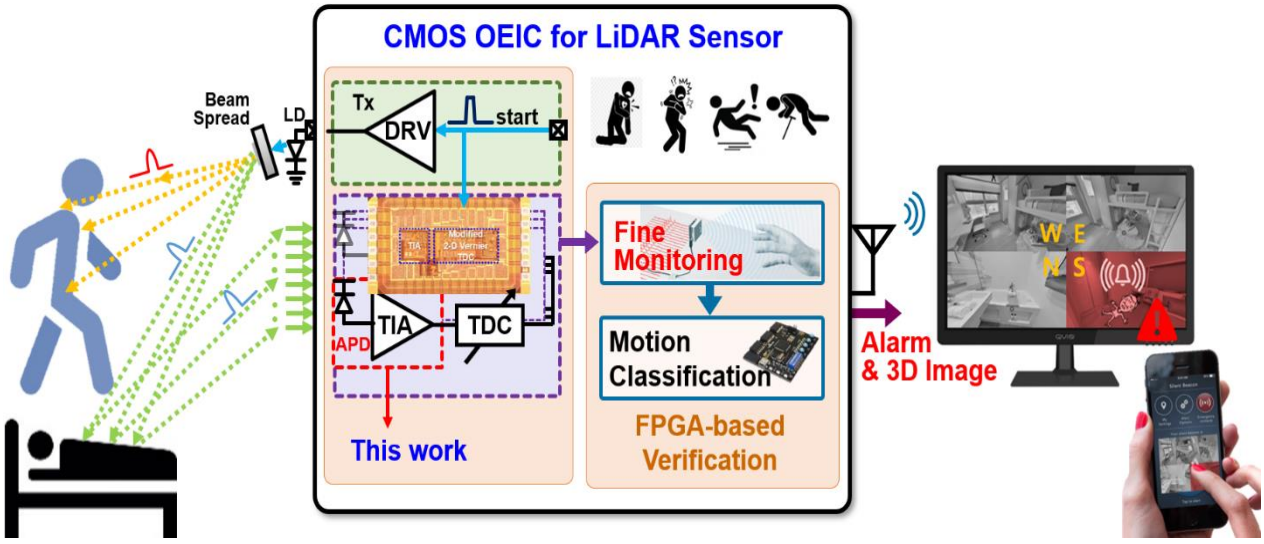


Fig. 2. Overview of the proposed LiDAR sensor for elder-care systems.

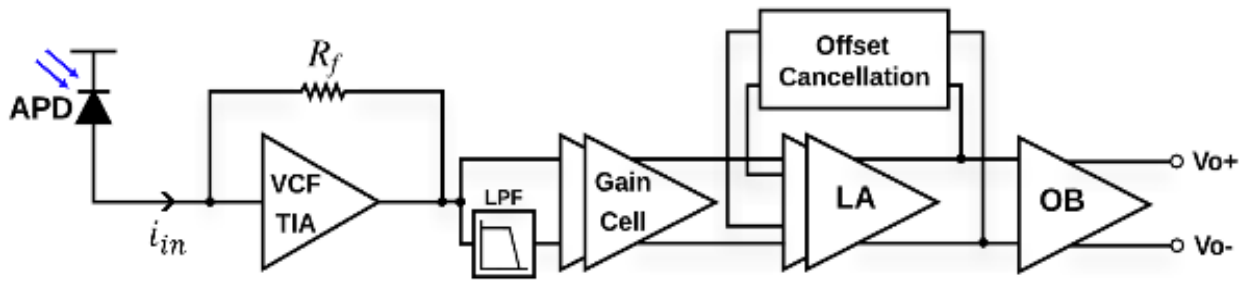


Fig. 3. Block diagram of the proposed OEIC AFE Rx.

capacitance circuits in order to guarantee a wide bandwidth with a proper gain. It is well known that the gain of a conventional differential pair cannot be increased indefinitely with a large load resistor even with the help of a negative-resistance stage. Certainly, the negative-capacitance helps to extend the bandwidth by reducing the effect of the output node capacitance [8].

The DC voltage offset cancellation network consists of a passive RC circuit cascaded by an amplifier, thus preventing the output voltage offset occurred from the excessive amplification otherwise. In this work, the corner frequency is set to several kilohertz to lessen the drooping.

Finally, f_T-doubler is exploited as the OB to halve the large parasitic capacitance yielded from a large tail current-source and also to match the output impedance to 50 Ω.

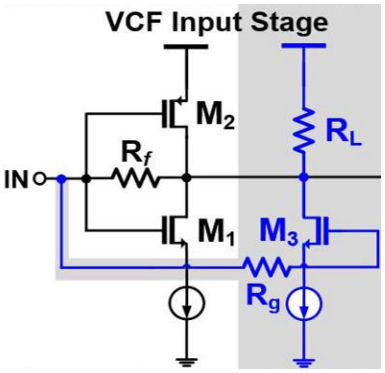


Fig. 4. Schematic diagram of the VCF-TIA

B. Simulation Results

Fig. 5 shows the chip layout of the proposed 4-channel OEIC Rx array which occupies the area of 2.0 x 2.5 mm2 including I/O pads. Circuit simulations were conducted by utilizing the model parameters of a standard 180-nm CMOS process. Fig. 6 depicts the simulated frequency response of the proposed OEIC Rx, obtaining the transimpedance gain of 96 dBΩ and the bandwidth of 780 MHz even with 3-pF photodiode capacitance. The input-referred RMS noise current is estimated to be 142 nA_{rms}, which corresponds to the noise current spectral density of 5.08 pA/$\sqrt{Hz}$.

Fig. 7(a) illustrates the simulated eye-diagrams of the proposed oRx with 30μA_{pp} PRBS input currents at different input data rates of 100 Mb/s, 400 Mb/s, 700 Mb/s, and 1 Gb/s, respectively.

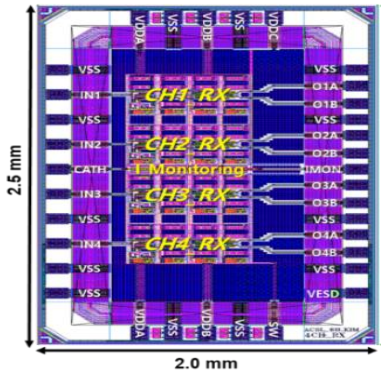


Fig. 5. Floor plan of the proposed OEIC AFE Rx array.

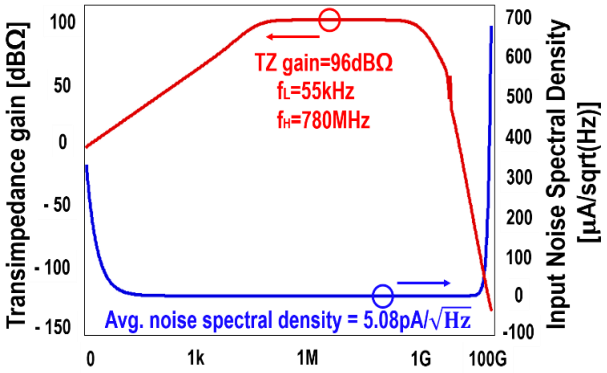
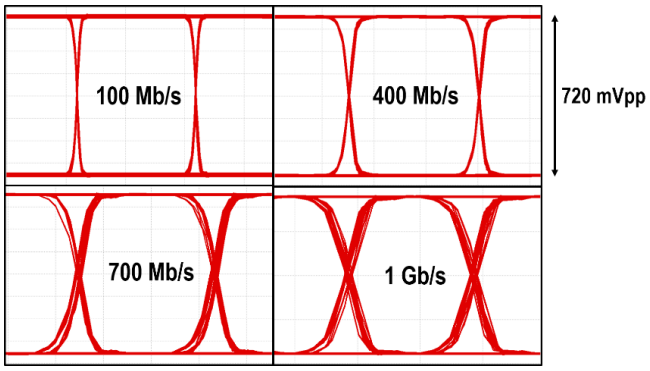
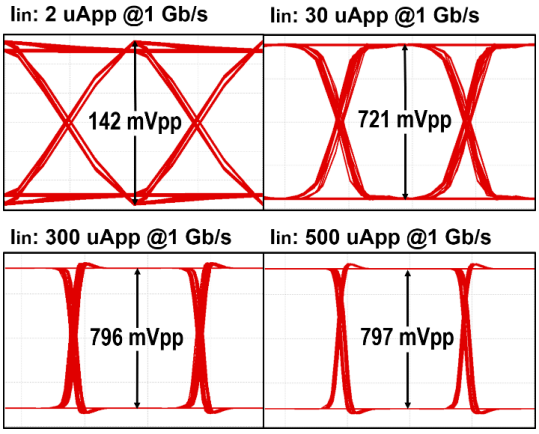


Fig. 6. Simulated frequency response of the proposed OEIC Rx.



(a)



(b)

Fig. 7. Simulated eye-diagrams: (a) at different input data rates with 30μA_{pp} PRBS input currents, (b) with different input amplitudes at 1-Gb/s

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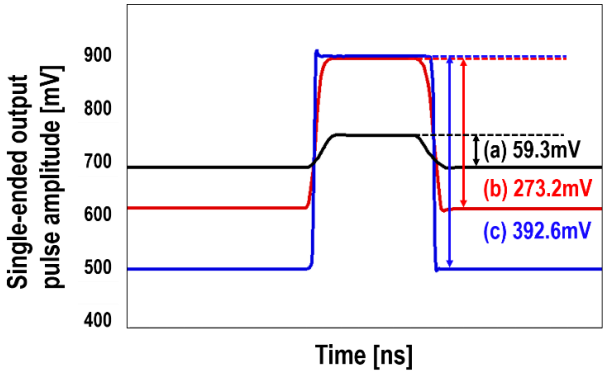

Fig. 8. Simulated transient output voltage pulses of the proposed OEIC Rx for (a) 2 μA_{pp} (b) 30 μA_{pp} (c) 300 μA_{pp} input pulses with a 5-ns pulse width, respectively.

TABLE I. Performance comparison of the proposed OEIC Rx array with prior arts

Parameters	**This work**	**[9]**	**[10]**	**[11]**
Supply Voltage	1.2 V	1.2 V	1.8 V	3.3 V
# of channel	4	1	1	1
TZ Gain	96 dBΩ	78 dBΩ	86 dBΩ	100 dBΩ
Bandwidth	780 MHz	640 MHz	281 MHz	450 MHz
Noise current spectral density	5.08 pA/$\sqrt{\text{Hz}}$	4.7 pA/$\sqrt{\text{Hz}}$	4.68 pA/$\sqrt{\text{Hz}}$	2.59 pA/$\sqrt{\text{Hz}}$
Power Dissipation per channel	29.2 mW	114 mW	200 mW	6.6 mW

Fig. 7(b) shows the simulated eye-diagrams at 1-Gb/s PRBS input currents with different input amplitudes of 2 μA_{pp}, 30μA_{pp}, 300μA_{pp}, and 500 μA_{pp}, respectively. It is clearly seen that the proposed oRx achieves wide and clean eyes with relatively wide dynamic range.

The DC voltage offset cancellation loop helps to relieve the notorious pulse width distortion (PWD) effect until when the input currents of less than 300μA_{pp} are generated from the optical detector (APD). For larger input currents than 300 μA_{pp}, the PWD can be controlled further by exploiting an automatic gain control (AGC) loop.

Fig. 8 depicts the simulated output pulses of the proposed oRx at its single-ended output, where the amplitudes of output voltage pulses are 59.3 mV, 273.2 mV, and 392.6 mV for input current pulses of 2 μA_{pp}, 30μA_{pp}, and 300μA_{pp}, respectively, with a 5 ns pulse width and 1 ns rise/falling time. Table I summarizes the performance of the proposed OEIC AFE Rx array.

IV. CONCLUSION

The proposed 4-channel OEIC receiver array designed in a 180-nm CMOS technology can be applied for the applications of a linear LiDAR sensor. Since the multi-channel oRx array particularly integrates a 4-channel spatially modulated avalanche photodiodes, it can yield a number of advantages over a conventional LiDAR sensor, such as lower cost, simpler integration, smaller package parasitic, etc. Conclusively, it is certain that this work can provide a potential for a low-cost AFE solution for short and medium-range LiDAR sensors, especially to save single elders and/or dementia patients in cases of emergency.

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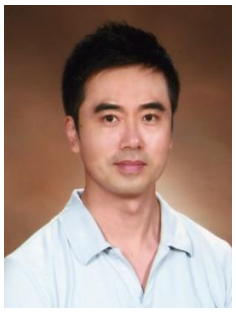
Ji Eun Joo received the B.S. degree in electronic and electrical engineering from Ewha Womans University, Korea, in 2020. She is currently working toward the MSc degree in the analog circuits and systems lab. at the same university. Her current research interests include silicon photonics, and CMOS optoelectronic integrated circuits and architectures for short distance optical application systems and sensor interface IC designs.

Myung Jae Lee received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2006, 2008, and 2013, respectively. From 2013 to 2017, he was a Postdoctoral Researcher with the faculty of electrical engineering, Delft University of Technology (TU Delft), Delft, The Netherlands, and in 2017, he joined the school of engineering, École Polytechnique Fédérale de Lausanne (EPFL), Neuchâtel, Switzerland, as a Scientist. Since 2019, he has been a Senior Research Scientist with the Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology (KIST), Seoul, South Korea, where he has led the research and development of next-generation single-photon detectors and sensors for various applications. His research interests include CMOS-compatible avalanche photodetectors and single-photon avalanche diodes and applications thereof (e.g., LiDAR, D-ToF, 3D vision, biophotonics, quantum photonics, space, security, silicon photonics, optical interconnects, etc.)



Sung Min Park received the B.S. degree in electrical and electronic engineering from KAIST, Korea, in 1993. He received the M.S. degree in electrical engineering from University College London, U.K., in 1994, and the Ph.D. degree in electrical and electronic engineering from Imperial College London, U.K., in May 2000. In 2004, he joined the faculty of the Department of Electronics Engineering at Ewha Womans University, Seoul, Korea, where he is currently a Professor. His research interests include high-speed analog/digital integrated circuit designs in submicron CMOS and SiGe HBT technologies for the applications of optical interconnects, silicon photonics, and RF communications.